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TABLE OF CONTENTS

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SEER, A SEquence Extrapolating Robot*

D. W. HAGELBARGER†

Summary—The success of computers in doing routine work formerly done by people suggests that a computer capable of adjusting itself to a changing environment might be desirable. Such a characteristic might be especially valuable to the telephone industry which must service large numbers of people having changing needs and desires. As a step in this direction a relay machine which plays a penny-matching game with human opponents has been built. The machine is described and its behavior against people and other machines discussed.

Introduction

THERE IS a game played by two school boys in which each of them chooses which side of a coin to expose. One of the boys tries to match the other. If both coins are the same, he wins; otherwise the other boy wins. This is a fair game since each boy wins for two of the four possible combinations. The theory of games says that, if you assume that your opponent is as smart or smarter than you are, a safe strategy is to play randomly with equal probability of heads and tails. This assures your not losing much since you can expect to win on the average half the time and come out even. This is, however, a rather staid approach. If you are smarter than your opponent, you should be able to guess which way he will choose and make your own choice so as to beat him more than half the time. In "The Purloined Letter," Edgar Allan Poe describes a boy who was successful at this game by assuming his opponent's facial expression and observing what he thought with this expression. This paper describes a relay machine built to play this game with human opponents. Rather than playing safe the machine tries to outwit its opponent and thereby win more than half the time. It has achieved a limited amount of success. Out of 9,795 plays against visitors and employees at Bell Telephone Laboratories, it has won 5,218 times and lost 4,577. The odds against the machine's getting this large a lead by chance alone are about 10 billion to one. These figures, however, should not be taken too seriously as there are several effects which bias them one way or the other. Some players use a simple sequence that the machine can beat just to see how fast it "catches on." This tends to make the machine's score higher than it should be. On the other side are people who cheat the machine to see how it behaves when losing. Also people who are consistently beat by the machine refuse to play it very many times, while people who come out even or win will tend to play it a long time. In general, the runs are too short; the machine spends about the first half of each game playing randomly while it is gathering data.

The Game

The front panel of the machine contains:

machine ready lamp
machine play button
plus lamp
minus lamp
opponent's play key
scoring lamps.

The machine plays first so that the player knows it is not cheating. When the machine ready lamp is on, the player announces whether he is going to play plus or minus. (The machine cannot hear.) He then pushes the machine play button and the machine lights either the plus or the minus lamp indicating its play. The player then indicates his choice on the opponent's play key. If both choices are the same, the machine wins; if they are different, the player wins. The machine records the score and is ready to play again.

Response to Simple Periodic Sequences

There are four periodic sequences which the machine can recognize and predict without making any errors once it has caught on. These are:

$$+ + + + \cdots$$
$$- - - - \cdots$$
$$+ - + - + - \cdots$$
$$+ + - - + + - - \cdots$$

On most short periodic sequences the machine wins somewhat more than half the time. It tends to recognize a certain part of the sequence each time it occurs even though it cannot remember the entire sequence. Some sequences cause the machine to come out even. I do not know of any periodic sequence which will beat the machine.

Fig. 1 shows a series of learning curves for the machine. The net score is plotted against the play number. The machine was cleared at the beginning of each curve and then the series $++--++--\cdots$ was played against the machine until inspection of the internal memory of the machine showed that it had recognized the sequence and would make no more errors. This point is marked with a *V* on each curve. The phase of the sequence was then shifted by inserting an extra symbol and the sequence continued until inspection of the memory showed that it has assimilated the phase change and would make no more errors. This point is again marked with a *V*. On the average, it takes the machine about 21 plays to recognize this sequence and 7 plays to assimilate the phase change.

Raison d'Être

Why build such a machine? The game which it plays is really not a very exciting one and probably has little

* Original manuscript received by the PGEC, October 28, 1955.
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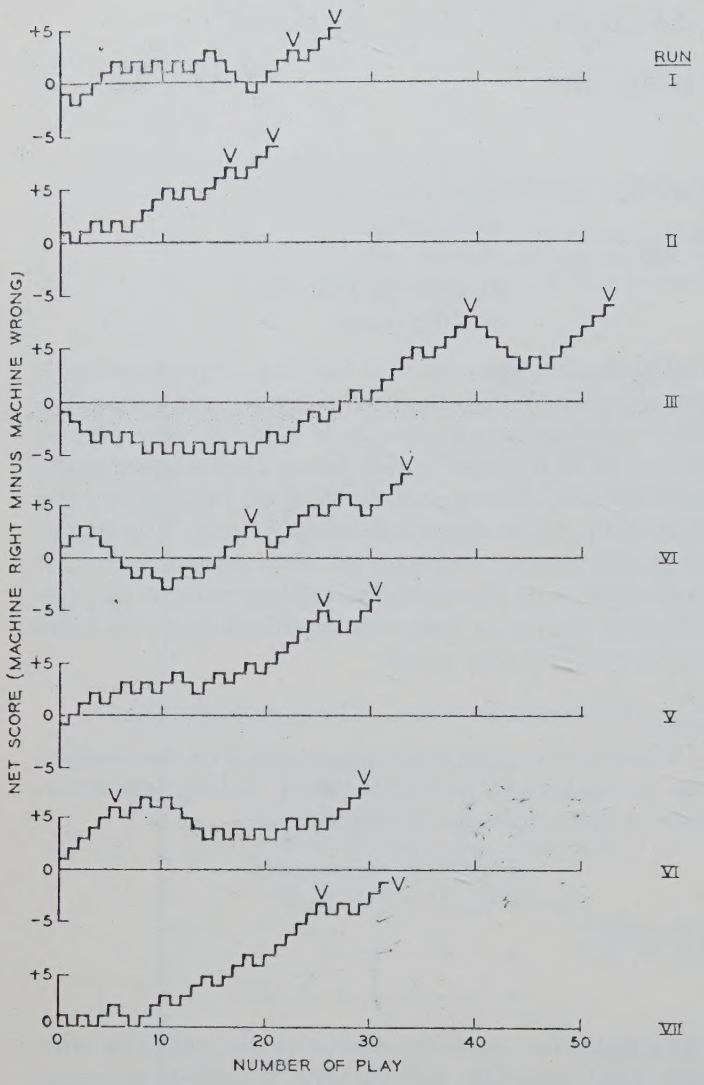


Fig. 1—Learning curves for $++--++--\ldots$

$++++\cdots$
$----\cdots$
$+-+-\cdots$

and having learned them quickly shift among them with few errors. It happens that these three sequences will all fit into the machine's memory with little conflict. Fig. 2 shows this experiment. As before, the symbol *V* indicates that examination of the internal memory reveals that the machine has "learned" the sequence and will predict it indefinitely without error, if desired. The machine was cleared and started with $++\cdots$ which it learned at *A*. It took 4 errors and 9 plays for it to switch to $----\cdots$ at *B*. It was able to return to $++\cdots$ at *C* with 2 errors and 7 plays. It now had a run of bad luck playing randomly and losing 7 plays in a row, but by *D* it had learned $+-+-\cdots$ in 27 plays with 16 errors. It returned to $++\cdots$ at *E* with 1 error and 4 plays, back to $+-+-\cdots$ at F with 2 errors and 5 plays, and so on. From *D* on it shifted among the three sequences with 1 or 2 errors and 4 to 5 plays per shift. Fig. 3 repeats the same experiment which is similar except bad luck after *C* is missing.

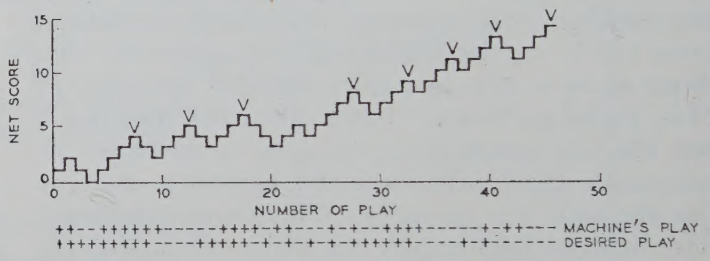


Fig. 3—Experiment of Fig. 2 repeated.

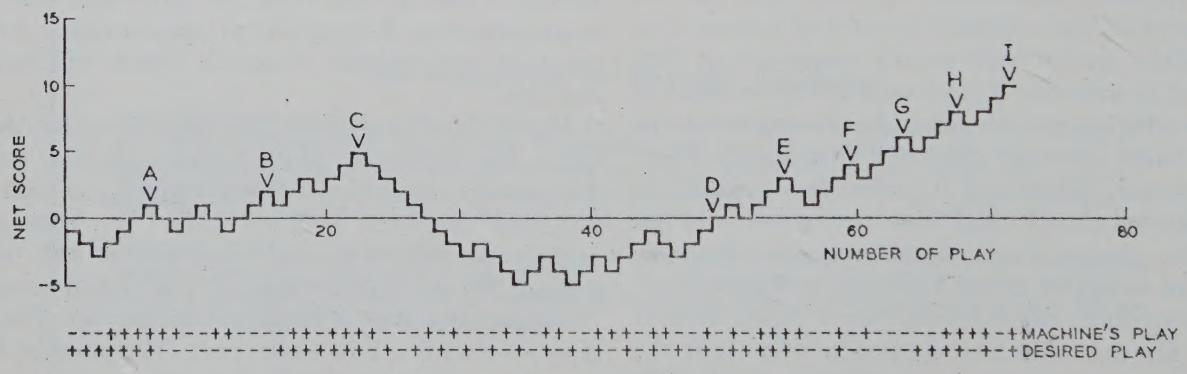


Fig. 2—Learning curve for three sequences.

or no commercial value. By relabeling the panel of the machine we can change it from an adversary to a servant which is trying to please the operator. In fact, the machine was first conceived of as an environment-adapting machine and was suggested by a proposal of J. R. Pierce for a music-composing machine. This environment-adapting behavior will be illustrated by having the machine simultaneously learn three sequences:

As machines get more and more complicated, it seems likely that not only routine matters but some things which we now call thinking[1] will be done by machine. For instance, in a telephone exchange there always ap-

[1] Some people prefer to stop calling it "thinking" as soon as a machine does it. Most of us agree that it is a higher form of intelligence for Newton (or Leibnitz) to invent The Calculus than it is for a school boy to learn it, but is the school boy thinking?

pear to be some jobs for which human operators are required. As telephone systems get more complicated the routine jobs will all be done by apparatus, leaving those requiring judgment and originality. Yet with the increasing use of higher speed devices it is getting harder to connect the person efficiently to the system. A person may easily be the bottleneck in a system which works at the rate of a million pulses per second. It is said that the reason people have been so successful evolutionwise is the ability of people to adjust to a wide range of environments. The ability of a machine to adjust itself to a changing environment will surely be desirable. A new toll alternate routing system is designed according to the measured statistics of the telephone system. If the statistics change the toll system must be redesigned and yet the new system itself may cause the statistics to change. We can imagine an alternate routing system which chooses alternate routes on a basis of how satisfactory previous choices were. Such a system could follow changing statistics.

It is possible, if not probable, that it would be economical to design a telephone central office to measure traffic and adjust itself accordingly. It might observe that most calls from the business district occur during the day and more calls from the residential section during the evening, and connect its apparatus accordingly, yet it would be able to readjust itself if a large fire occurred in the business section during the night.

Perhaps in an extremely complicated situation it might be easier to design a machine which learns to be efficient than to design an efficient machine as such.

Of course we are a long way from anything as sophisticated as this. To give an idea of how much intellectual activity to expect from the out-guesser, consider that a man has 10^{10} neurons, the very dumbest army ant has 200 neurons, and this machine has less than 100 relays.

Strategy[2]

The strategy of the machine is based on two assumptions:

a) The play of people will not be random. They will be influenced by training and emotions so as to produce patterns in their play. For example, some people after winning twice, say, will tend to "stick with their luck." Others will feel they should not "push their luck" and change. In either case, if they are consistent, the machine should catch them.

b) In order to make it hard to beat, the machine should have its output correlated only when it is winning and play randomly when it loses.

To make its play symmetrical in + and − the machine does all its calculating in terms of whether this play should be the *same* as or *different* from the last play.

[2] For a more detailed description, see Appendix I.

What we will call the "state of play" of the machine is determined by three things:

a) whether it won or lost last play
b) whether it won or lost play before last
c) whether it played *same* or *different* last time.

This information is stored in the state of play relays (see Fig. 4). There are 8 states that the machine can have. Each of these has its own memory register.

At the beginning of any play, the computer is connected to the appropriate memory register by the state of play relays. The memory stores two kinds of information:

a) Should the machine play *same* or *different* in this state in order to win?
b) Has the machine been winning in this state?

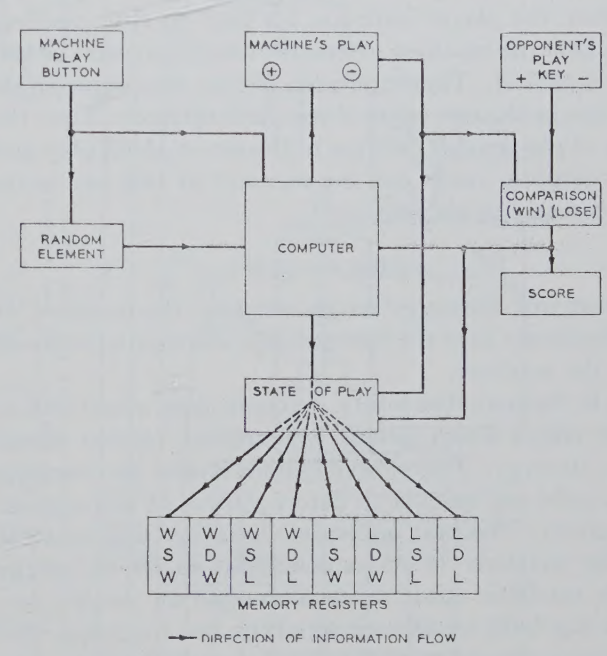


Fig. 4—Block diagram of SEER.

The a) part of the memory is controlled by a reversible counter which starts at zero and can count up to +3 and down to −3. At the end of each play, if the machine should have played *same*, one is added to the counter. If it should have played *different*, one is subtracted. The counter will thus contain the number of times the machine should have played *same* in that state minus the number of times it should have played *different*. The stops at +3 and −3 in effect make the machine forget ancient history. The exact logic of the b) part of the memory is rather complicated when written out in words, but it roughly corresponds to remembering whether the machine has won both, one, or neither of the last two plays in that state.

When the player pushes the machine play button two actions are started:

A random number 1, 2, 3, or 4 is selected by the random number generator (this is determined by the

position of a commutator at the instant the button is pressed).

The computer determines the machine's play from the following rules:

If the machine has lost the last two times in the present state, it plays randomly with equal odds on *same* and *different*.

If the machine has won one of the last two times in this state, it has three-to-one odds that it will follow the instruction in the a) part of the state memory.

If the machine has won both of the last two times in this state, the machine must follow the instruction in the a) part of the state memory.

When the player indicates his play on the opponent play key, the machine calculates whether it won or lost and scores it. The computer makes the appropriate changes in the two parts of the state memory. Then the state of play circuit changes to the new state of play and the computer reads out the memory of this new state and is ready to play again.

Miscellany

There are strategies[3] which will beat the machine. It can be shown that the best possible strategy wins 60–40 over the machine.

C. E. Shannon has built a machine using about half as many relays which follows a simplified version of the same strategy. The simplifications make his machine more agile and quicker to detect a trend at the expense of security. The best opponent's strategy will beat the smaller machine 75–25 as compared to 60–40 for the larger machine. After much discussion an umpire machine was built which connected the two machines, and they were allowed to play several thousand games. The agility of the small machine triumphed, and it beat the larger one about 55–45.

Appendix I

Circuit Logic and Operation

(To be read one word at a time with one finger on the text and one finger on the circuit diagram, Fig. 5.)

The operation of the circuit will be described by following through one play in detail. At the start of a play stepping switch 3 is in position 20. Since stepping switch 3 controls the sequencing, repeated reference will be made to its position. Relays will be referred to by letter only without saying "relay" every time.

Position 20—Closing the machine play pushbutton operates S. S locks up. R_1 and R_2 lock up in one of their four possible states, according to the position of the commutator when S operates. R_0 also locks up and converts the commutator to a pulse source for stepping switch 3.

Positions 21–25, 1, 2—Empty.

Position 3—N operates and connects WZ_4 to the input of the tree on R_1 and R_2. If a minus comes through the tree, WZ_4 changes state and DS locks up. (WZ_4 is the machine's play; a minus pulse makes it play *different*. DS remembers if WZ_4 played *different*.)

Position 4—N releases, M operates and locks up, lighting either the + or − lamp, removing the pulses from stepping switch 3, and connecting minus to the opponent's play key circuit. The machine remains in this state until the opponent's play key is moved to either + or − causing W or L to operate and lock up. Either the "machine wins" or the "player wins" lamp is lighted and a count is put in either the W or L message register. The opponent's play key is removed from the circuit and pulses from the commutator are again applied to stepping switch 3.

Position 5—A count is put into one of the non-random W or L message registers if either PW_1 or PW_2 (or both) is operated.

Position 6—C_0 operates and locks up. This disconnects $WZ_{1,2,3}$ and the PW circuit from the memory register corresponding to the present "state of play" and clears this memory register. It also operates and holds D if DS and W agree. (Play *different* and win or play *same* and lose.)

Position 7—The previous wins (PW_0, PW_1, PW_2) circuit, which controls the odds in using the random element, is pulsed. If neither PW_1 nor PW_2 is operated the odds are 2:2 and the play is random. If only one of them is operated the odds are 3:1 in favor of following the play corresponding to the sign of the number in $WZ_{1,2,3}$. If both PW_1 and PW_2 are operated the machine must play according to $WZ_{1,2,3}$. Whenever the play agrees with the instructions in $WZ_{1,2,3}$ and the machine wins, the odds are increased. Whenever the play agrees with the instructions in $WZ_{1,2,3}$ and the machine loses, the odds are decreased. For other cases the machine is designed pessimistically (to make it harder to beat). It never increases the odds unless it wins; however, it may leave the odds unchanged. For example, if PW_1 only, say, is operated and $WZ_{1,2,3}$ has a negative number (*different*) in it, the machine has 3:1 odds in favor of playing *different*. If the machine plays *different* the odds are increased to 4:0 if the machine wins and decreased to 2:2 if it loses. If the machine plays *same* the odds are not changed if it wins or loses.

Position 8—A pulse is applied to $WZ_{1,2,3}$ which counts up or down according to whether D is released or operated. The counter has end stops at +3 and −3.

[3] Appendix II.

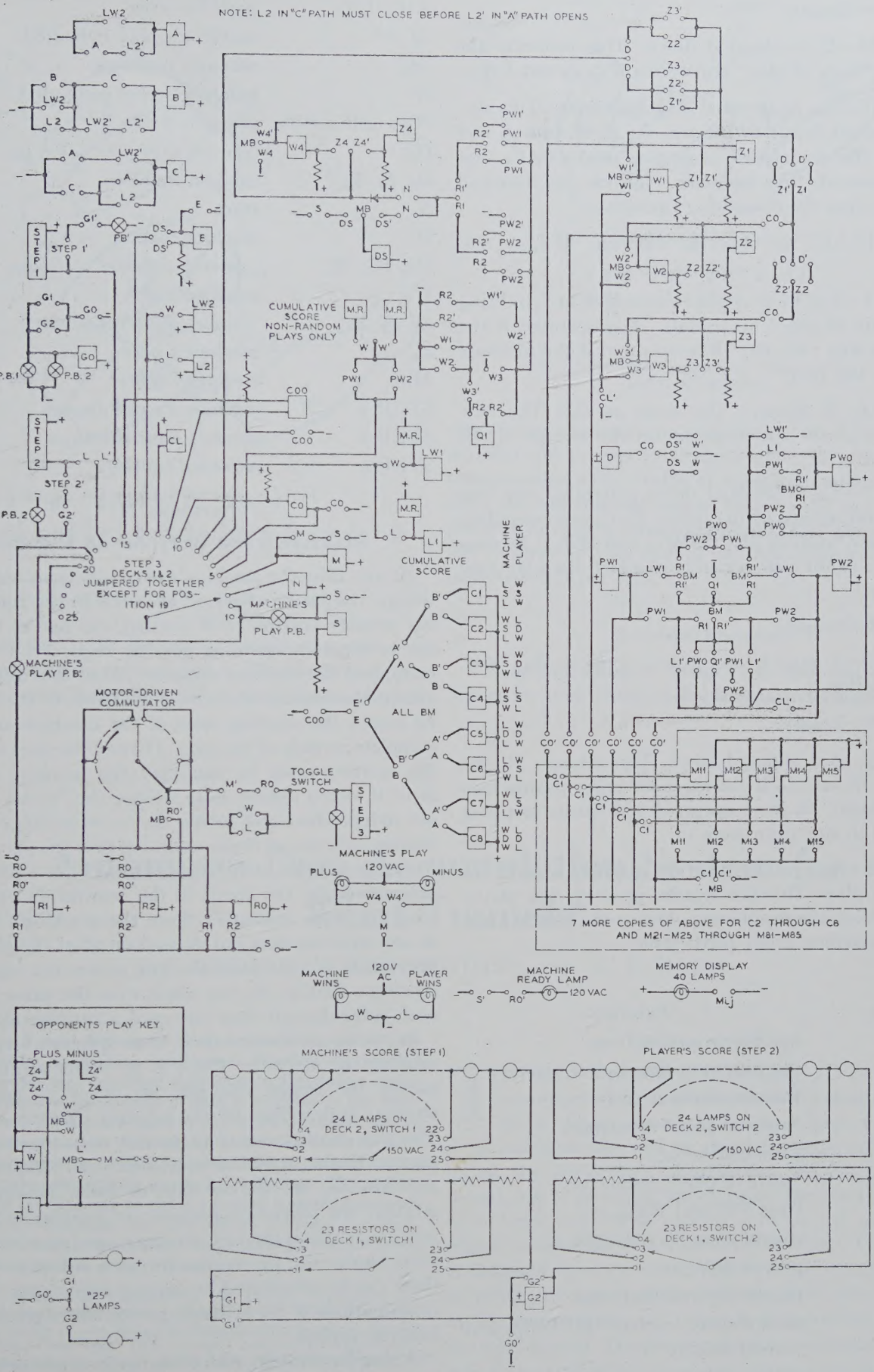


Fig. 5—Circuit diagram of SEER.

Position 9—Empty.

Position 10—C_0 is shunted down. This connects the present "state of play" register to $WZ_{1,2,3}$ and $PW_{1,2}$.

Position 11—C_{00} is operated and locked up. This disconnects the input to the tree on A, B, and E and releases the one of the connecting relays C_1–C_8 that was operated. The memory registers are now all isolated from the computing circuits.

Position 12—CL is operated clearing $WZ_{1,2,3}$ and $PW_{0,1,2}$.

Position 13—A pulse is applied through W or L to bring the "state of play" up to date. A is operated if the machine won this play. B is operated if the machine won the last play.

Position 14—E becomes the same as DS. The new "state of play" is now set up on the tree on A, B, and E.

Position 15—C_{00} is shunted down activating the tree and operating one of the relays C_1–C_8 corresponding to the new "state of play." $PW_{1,2}$ and $WZ_{1,2,3}$ become the same as the new registers to which they are now connected.

Position 16—Empty.

Position 17—A pulse is sent to one of the scoring stepping switches.

Position 18—Empty.

Position 19—S is shunted down. This releases R_1, R_2, M, DS, W, and L. If the machine's play pushbutton is not closed, R_0 stays operated and causes stepping switch 3 to step once more to:

Position 20—R_0 is released and the machine is ready for the next play. This last feature prevents the player from holding the pushbutton down and thereby making the machine's play predictable.

Résumé

Relay	*Function*
A	machine won last time
B	machine won time before last
C	transfers from A to B
C_{00}	"state of play" disconnect
C_0	main connector
C_1–C_8	"state of play" connectors
CL	clear PW and $WZ_{1,2,3}$
D	should have played *different*
DS	played *different*
E	played *different* last time
G_0, G_1, G_2	score display, control "25" lamps and reset display
L, L_1, L_2	machine loses
LW_1, LW_2	machine wins
M	machine's play indicated
M_{ij}	memory registers
N	machine's play computed
PW_0, PW_2, PW_2	previous wins
Q_1	counter says play *same*
R_0, R_1, R_2	random number
S	start
W	machine wins
W_1, W_2, W_3	*same—different* counter
W_4	machine's play
Z_1, Z_2, Z_3	*same—different* counter
Z_4	machine's play
M.R.	message register
STEP 1	machine's score display
STEP 2	player's score display
STEP 3	sequence control

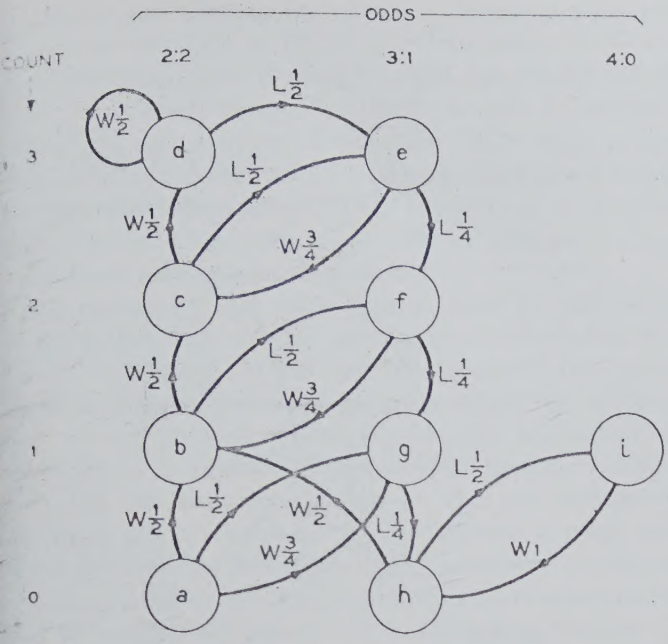
Appendix II

Strategies for Beating the Machine

At any time the machine's play is determined by four things: the "state of play," the odds in the corresponding memory register (PW circuit), the sign of the number in the corresponding counter register ($WZ_{1,2,3}$ circuit), and the random element. All of this information except the random element is available to the player if he knows the starting state of the machine and keeps complete records of the play. (Even if he does not know the starting state he can play the machine so as to force it into a known state.) Since the "states of play" are independent and follow the same strategy, we will discuss only one of them assuming that the player keeps 8 records, one for each "state of play." Let a substate be determined by the count in the counter and the odds. (See Fig. 6 for example.) Since the machine's behavior in any substate does not depend on what the player did previously in that substate, the player can use a pure strategy, that is, he can always do the same thing in each substate and does not need a random element.

It can be shown that there is an optimum strategy for beating the machine. There is no better strategy and, except for trivial changes, no other as good. The strategy is described by the substate diagram of Fig. 6. The player plays so as to permit only the transitions shown. Each transition is labeled with its probability and whether the player wins or loses. Following this strategy the player's expectancy of winning is 3/5. The proof that this is the best strategy consists of examining what choice the player has for each substate. Most of these can be eliminated by general arguments. Then all combinations of the remaining choices are tried and the best one picked.

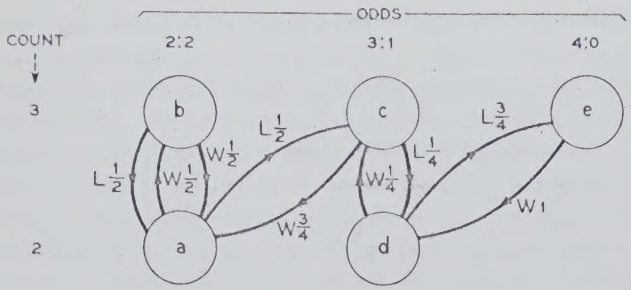
A simpler strategy which beats the machine is to play the opposite to what you did the last time for each of



$$W = \frac{1}{2}a + \frac{1}{2}b + \frac{1}{2}c + \frac{1}{2}d + \frac{3}{4}e + \frac{3}{4}f + \frac{3}{4}g + \frac{1}{2}h + i$$
$$= \frac{1}{2}\frac{1}{30} + \frac{1}{2}\frac{1}{9} + \frac{1}{2}\frac{2}{9} + \frac{1}{2}\frac{2}{9} + \frac{3}{4}\frac{2}{9} + \frac{3}{4}\frac{1}{9} + \frac{3}{4}\frac{2}{45} + \frac{1}{2}\frac{1}{45} + \frac{1}{90}$$
$$= \frac{3}{5}$$

Fig. 6—Substate diagram for optimum strategy.

he eight states. With the proper initial state this follows the substate diagram of Fig. 7. The player's expectation of winning is 23/40 = .575. A machine for playing



$$W = \frac{1}{2}a + \frac{1}{2}b + \frac{3}{4}c + \frac{1}{4}d + e$$
$$= \frac{1}{2}\frac{3}{10} + \frac{1}{2}\frac{3}{20} + \frac{3}{4}\frac{1}{5} + \frac{1}{4}\frac{1}{5} + \frac{3}{20}$$
$$= \frac{23}{40}$$
$$= 0.575$$

Fig. 7—Substate diagram for "Opposite from last time" strategy.

this strategy against the outguessing machine was assembled and a run of 1,043 plays taken. (The outguesser was provided with a table of random numbers on tape since the commutator was no longer valid as a random element against another machine.) The strategy won 598 times or 57.3 per cent of the time compared with an expected 57.5 per cent.

Acknowledgment

The author wishes to thank C. E. Shannon and E. F. Moore for many helpful discussions and suggestions.

Automatic Data-Accumulation System for Wind Tunnels*

J. J. WEDEL†, A. HUNTINGTON†, AND M. B. BAIN†

Summary—A new high-speed data-accumulation system has been designed for a supersonic wind tunnel. The data are recorded on punched paper tape for direct input into an Electrodata digital computer. Extensive presentation of data is available to the wind-tunnel operators. All data are typed by an electric typewriter, and an automatic plotting machine plots several of the data words as functions of the independent-variable data word. Special codes to control the computer are automatically punched into the tape. The preliminary source of the data may be either manually operated keyboards or shaft-position digitizers. The new system increases the wind-tunnel pace, eliminates intermediate data handling before computation, and lowers the cost of data reduction.

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Introduction

THE JET Propulsion Laboratory (JPL) operates two supersonic wind tunnels and is constructing a third. These tunnels generate a large volume of data which are reduced by the digital-computing facility of the Laboratory. Equipment has been built to record, on a punched paper tape, the data obtained from force tests. The tape is suitable for use in the digital computer with a minimum of editing. The system is designed to work with a computer processing center in which the larger portion of computer time is taken up by computation for research programs other than the wind tunnel. The present data-accumulation system is to be expanded to a complete automation of pressure

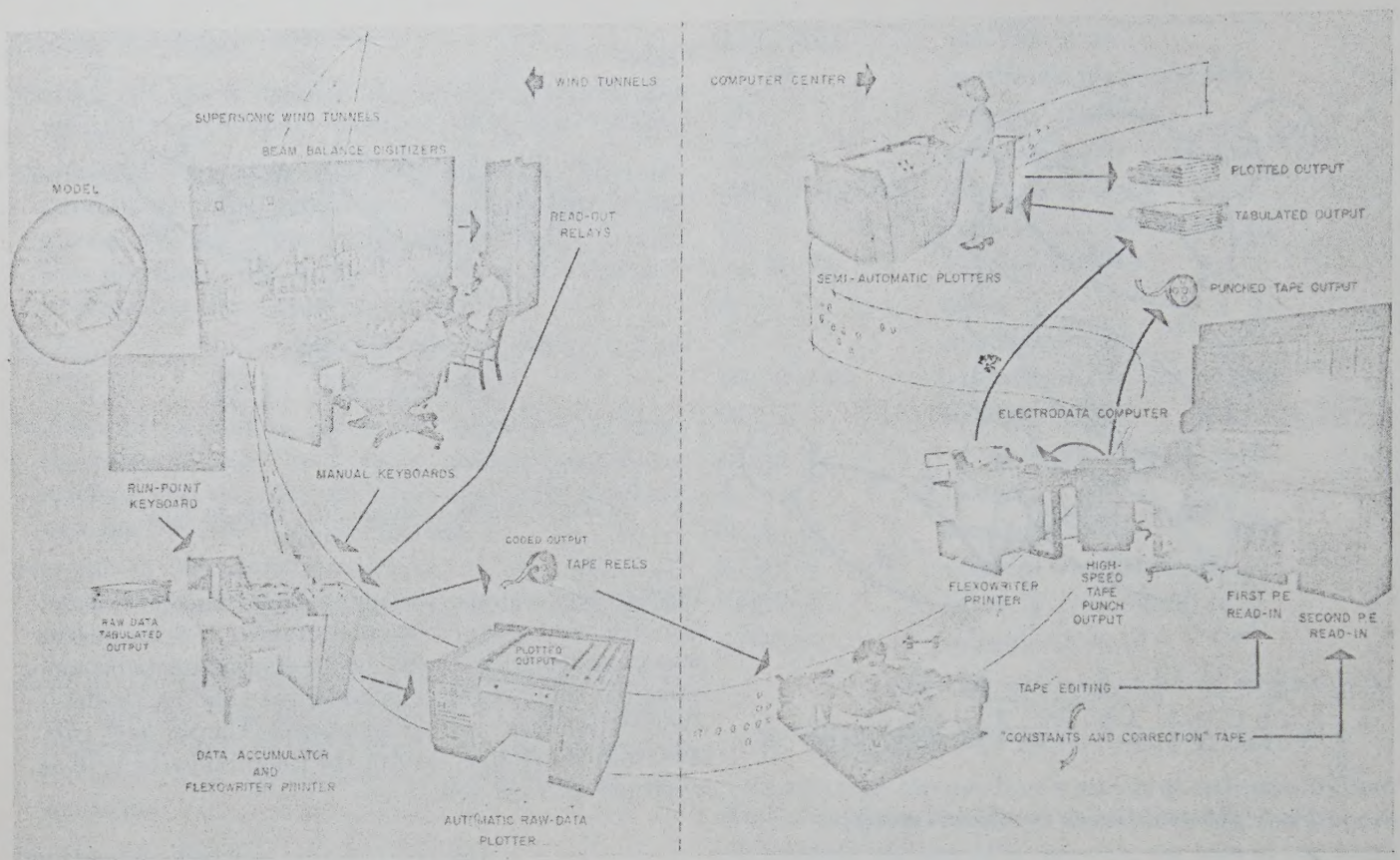

Fig. 1—Flow diagram of data-reduction system.

tests. The system developed has been effected at a minimum cost consistent with speed, reliability, and the accomplishment of necessary functions. It is a marked improvement in data-reduction service.

Wind-Tunnel Force Tests

In the supersonic wind tunnels, force tests are conducted by suspending an accurate model on a balance system. A typical balance uses various links and flexures to resolve a total of six components corresponding to the six possible degrees of freedom of a rigid body in space. Each component is sensed by a hydraulic device which produces a pressure used to position an automatic beam balance. The six beam balances have digital indicators for manual observation and also are equipped with automatic digitizers.

In addition to the force components, it is necessary to record other data to complete the tests. This supplementary information includes the model position, which is usually the independent variable, and also various pressures which define the operating conditions of the wind tunnel itself. At the present time, this information is inserted manually into the system by means of keyboards.

All of these raw data must be available for inspection by the wind-tunnel operating engineer. By examining the data, particularly its continuity, the engineer may sometimes detect malfunctioning of the data-handling equipment, the tunnel, or the model itself; and he may also plan the future course of the test.

The reduction of force-test data primarily requires a change in coordinate system for the force components. The data must be converted from the balance coordinate system to a system selected by the user of the test results. The process requires various rotations, translations, and changes of scale which also include the effects of gravity on the model, of elastic deflections of the balance-model system, and minor imperfections in the balance system.

The optimum reduction scheme from the standpoint of the wind-tunnel personnel would be a computer connected directly to the wind-tunnel instrumentation, producing reduced coefficients immediately after data are obtained. Such a system would be uneconomical at JPL because the wind tunnel only occupies about 25 per cent of the computer time. The larger part of the computer load is concerned with a number of problems related to the major research and development programs of the Laboratory. Under these circumstances, it has proven satisfactory to present reduced data to the wind-tunnel personnel on a daily basis. Such service requires that the test constants and exact results desired be made known to the computing staff one day before the test begins, so that suitable modifications may be made to the standard computer program. If raw data are presented to the computing group at noon, the wind-tunnel engineer will receive a listing of reduced coefficients the following morning. The details of the data-reduction process are the subject of another paper to be presented elsewhere.[1]

[1] W. R. Hoover, "Wind-Tunnel Data Reduction Using Paper-Tape Storage Media." A paper presented at the meeting of the Association for Computing Machinery, September 1955, in Philadelphia, Pa.: (Accepted for publication in *Jour. Assn. Computing Machinery*.)

Data-Accumulation System

The major components of the data-accumulation system are depicted in Fig. 1 (previous page). Information is obtained from the two types of data source: automatic digitizers attached to the hydraulic tunnel balances and manually set keyboards. These sources are sequentially interrogated by an automatic scanner which punches the information into a paper tape. Extensive presentation of raw data is provided by an electric typewriter and an automatic plotter.

Up to twenty-four data sources may be connected to the system but the scan may be terminated after any desired number of sources have been scanned. Operating speed is thereby increased for tests which require that only a small amount of data be recorded. Identification of the data is provided by a special keyboard which contains two numbers known as the run and point numbers. Each scanning cycle constitutes a point and the point number is automatically increased by one at the end of the cycle. A collection of points corresponding to various values of the independent variable is known as a run. The run and point numbers are punched into the tape as the first word of the point. The special run-and-point-number keyboard (Fig. 2) is equipped

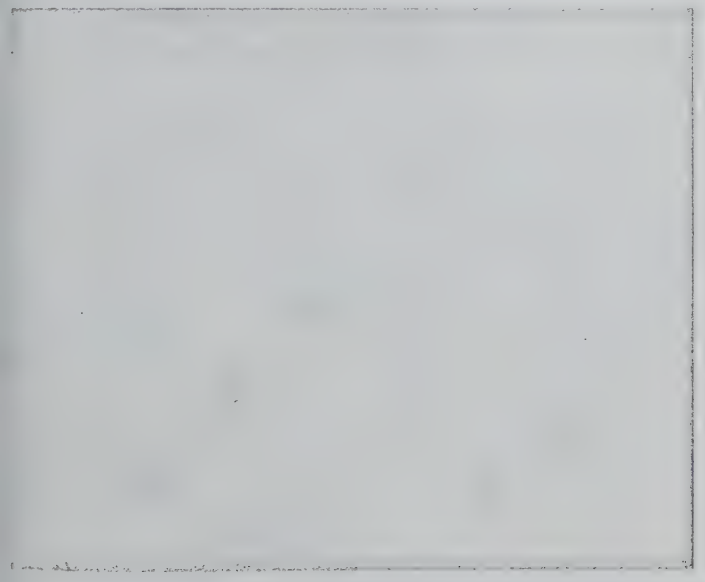

Fig. 2—Photograph of run-and-point number keyboard.

with illuminated keys so that it may be used as an indicator by the wind-tunnel personnel. Scanning is accomplished at a basic speed of two data sources per second, and is limited by the punch speed. The speed will be doubled in the future by installation of a high-speed punch.

In the course of a test, after the independent variable is changed, the keyboards are set by operators as soon as new stable operating conditions are established. When all keyboards are set, the digitizers are locked and the scanning cycle initiated. Because the digitizers are locked and input data cannot change, the tunnel operator may immediately proceed to change the independent variable to a new value. This procedure increases the over-all speed of data recording and reaches a maximum speed when the scanning time is equal to the time required to change tunnel operating conditions.

The raw data are typed by a Flexowriter[2] which reads the punched paper tape. By operating the Flexowriter from the tape rather than from the signals which operate the punch, the probability of an incorrect tape with a correct listing is made very small. The tape also serves as a buffer storage between the punch and the raw-data Flexowriter. The Flexowriter is equipped with a special wide carriage, and all data from a scan are recorded on one line. The machine is also automatically started and stopped as explained subsequently.

Fig. 3 shows the data scanner and Flexowriter. The tape punch now in use is the regular punch supplied with the Flexowriter, but it is no longer electrically connected to the regular punch circuits. The high-speed punch will of necessity be mounted externally.

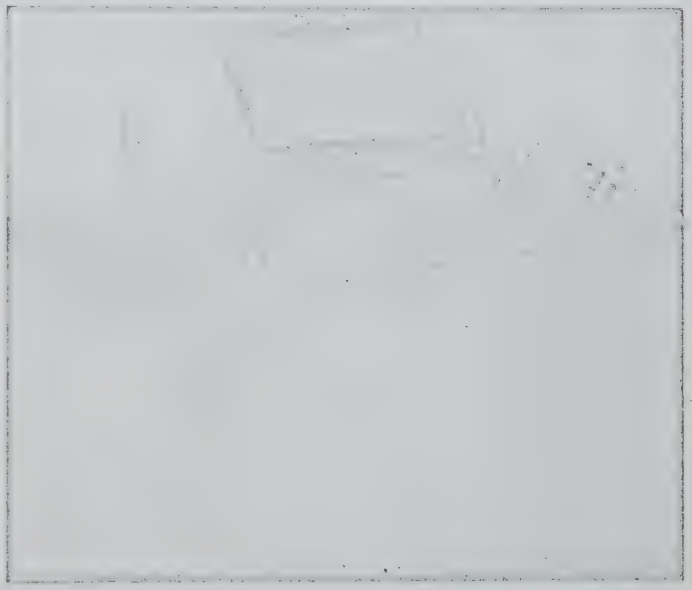

Fig. 3—Photograph of data-accumulation scanner and Flexowriter.

Although all data are listed by the Flexowriter, only selected items are plotted by the automatic plotter. By means of switches, 13 words, not necessarily consecutive, can be selected out of the maximum of 24 words which are punched during one scan. The automatic plotter treats the first of these words as the independent variable and plots the remaining 12 words as dependent variables. Separate scale and zero-position adjustments are available for all variables, and in addition it is possible to cause an offset in the position of the independent variable after a selected number of words have been plotted. The offset permits the format to consist of two groups of plots side by side. Plotting is accomplished on a 30×30-inch surface to an accuracy of 0.1 per cent. The speed is dependent on the excursion of the pen from point to point. The plotter is operated from the Flexowriter tape reader, and if words arrive too fast to be plotted, the reader and the Flexowriter

[2] Manufactured by Commercial Controls, Inc., Rochester, N. Y.

(but not the punch) are stopped to allow the plotter to catch up. A skillful operator can usually arrange the data so that the plotter does not slow down the Flexowriter except, possibly, when the position of the independent variable changes. A photograph of the automatic plotter is shown in Fig. 4.

Fig. 4—Photograph of automatic plotter.

The paper tape prepared by the data-accumulation system is used directly in the digital computer photoreader. A very small amount of editing may be required to correct keyboard punching errors. The tape is read into the computer on a run-by-run basis, and any information in addition to the raw data that is needed to process a run is inserted from a second input photoreader. Error corrections can, of course, also be read in through the second photoreader.

The right-hand side of Fig. 1 depicts the data-reduction functions that take place at the computing center. The computer output is obtained on a punched paper tape which is used to list reduced coefficients on a Flexowriter. The computer produces the output tape much faster than it can directly operate the Flexowriter, thus shortening the time that the computer itself is required to spend processing the data. The output tape can be listed at any time, including part of the maintenance period, that the Flexowriter is not required for direct output from the computer. Finally, some of the data are plotted with a keyboard-operated semi-automatic plotter.

Choice of Storage Medium

The choice of punched paper tape as a storage medium was made for several reasons. Magnetic tape was not used because of the cost and complication of the system. The final choice was between punched paper tape and punched cards.

The digital computer at the Laboratory uses punched paper tape for its input medium. Although card-input equipment is available from the manufacturer, it is costly and its use reduces the speed with which data can be inserted into the computer. At the originating end, paper tape also offers advantages. A serial card punch being too slow for data accumulation, a gang punch is necessary. The use of a gang punch requires a considerably more complicated data accumulator.

Another possibility is the use of card equipment at the wind-tunnel, in conjunction with a transcriber to punch paper tape for the computer. This procedure requires complicated and bulky originating equipment for cards at the wind-tunnel, as well as an investment in transcribing equipment. The transcription process also delays data processing and introduces a possible source of error. Another advantage of tape storage is that it is less bulky than card storage. Tape storage does possess the disadvantage of a relative inflexibility for editing, but the disadvantage has been minimized by data-processing procedures. Also, as noted earlier, the tape serves as a convenient buffer storage between fast punching and slower typing or plotting, thus eliminating the need for special equipment to serve this purpose.

Data-Accumulation Components

A block diagram of the scanner, including the keyboard connections, is shown in Fig. 5. The keyboards

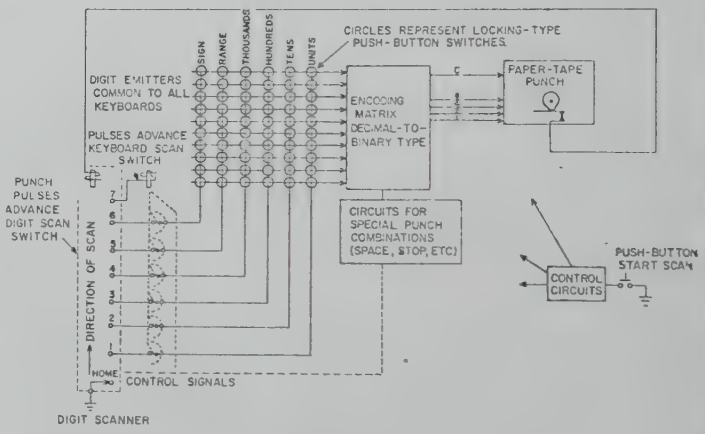

Fig. 5—Block diagram of scanner and keyboards.

are equipped with four decimal columns of locking keys, a three-valued range key, and a sign key. The range and sign digits are handled by the equipment as though they were decimal digits. The digitizers[3] are constructed in such a way that no mechanical contact is made except when a read-out signal is provided to them. This construction minimizes wear on the brushes and contact plate. The digitizer brush signals are decoded by a system of relays in such a manner that their output connections are identical to those of a keyboard.

Timing signals, controlled by the tape punch, cause the digit scanner switch to scan the six columns of a given keyboard sequentially and then advance the keyboard-stepping switch to connect the next keyboard to the system. The digit-scanner switch is a magnetic

[3] Manufactured by Coleman Engineering Co., Los Angeles, Calif.

counter[4] which is reset by a single pulse after each keyboard is scanned. After the scan has been completed at the selected final keyboard, the keyboard-stepping switch homes through its interrupter contacts. This last scan of the digit-scanner switch has two extra positions which punch a carriage return and a stop code into the tape. These codes control the raw-data Flexowriter and are ignored by the computer. The decimal digits from the keyboards are converted into binary-coded decimal digits in a diode encoding matrix, and the binary-coded digits operate the punch-control magnets.

Additional features have been provided in the data-accumulation system for operating convenience. The digital computer which processes the data requires a special word to be punched into the tape at the end of read-in, in order to transfer command to the computer. Punching of this word into the tape is manually initiated by the tunnel operator, but carried out automatically while the scanner resets its point register at the end of a run. Means are available for tagging certain words punched on the tape to indicate that they are to be specially processed by the computer.

The Flexowriter used for typing raw data is a special model FL using the binary-coded decimal tape code employed by the computer. The tape punch has been disconnected from the Flexowriter circuit and reconnected to the data scanner. Connections have been brought out from the tape reader to operate the raw-data plotter. The Flexowriter is started simultaneously with the scanner and reads tape until it encounters the stop code punched at the end of the scan. This cycle of operation was chosen to make it possible to eventually use a high-speed punch, separate from the Flexowriter, which will punch tape at twice the speed of the present punch. When the high-speed punch is in operation, the Flexowriter will catch up with the punch during the interval between scans. A tension-operated device emits sufficient blank tape at the end of a scan to permit the stop code to enter the tape reader.

Fig. 6 is a block diagram of the automatic plotter.

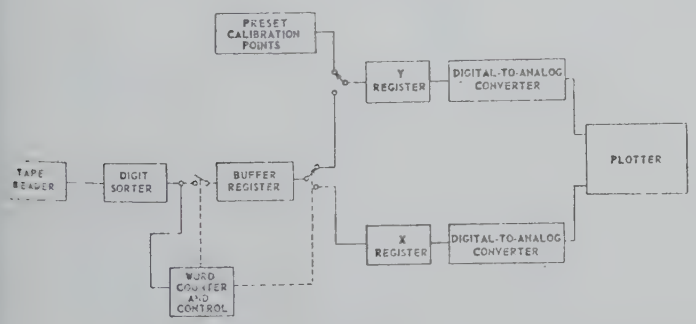

Fig. 6 – Block diagram of automatic plotter.

The number from the tape reader is changed from serial into parallel form by the digit sorter, and the selected words are sent to the buffer register. The first selected word is transferred from the buffer register to the X register; the remaining words go to the Y register. The buffer is interposed between the reader and the plotter registers so that the tape reader need not be stopped during the plotting operation. If, however, a selected word arrives in the buffer register before the plotter registers are ready to receive it, the tape reader is temporarily stopped.

Selection of desired words is accomplished by control switches in conjunction with a word counter. Standard six-digit wind-tunnel word consists of algebraic sign, a three-valued range digit, and four data digits. Either first three or last three data digits are plotted.

A modified Variplotter[5] performs the plotting operation. The Variplotter is a null-seeking-servo analog device. After its two servos have reached the null position, the pen is dropped for a short time to produce a dot. The pen is then raised and the plotter moves to a new point. One axis of the Variplotter consists of a relatively heavy arm; the other axis is a lighter pen-carriage assembly which moves rapidly on the arm. The slow, heavy arm has been chosen for the X axis, the independent variable, because it only moves twice during a complete plotting cycle for one data point.

The balancing circuits of the Variplotter have been placed in a bridge circuit. Part of this bridge consists of the feedback potentiometer, and the other part is a series of fixed resistors which are connected into the circuit by means of relays. This latter part of the bridge is a digital-to-analog converter; the relays are operated from the X and Y registers. (See Fig. 7).[6]

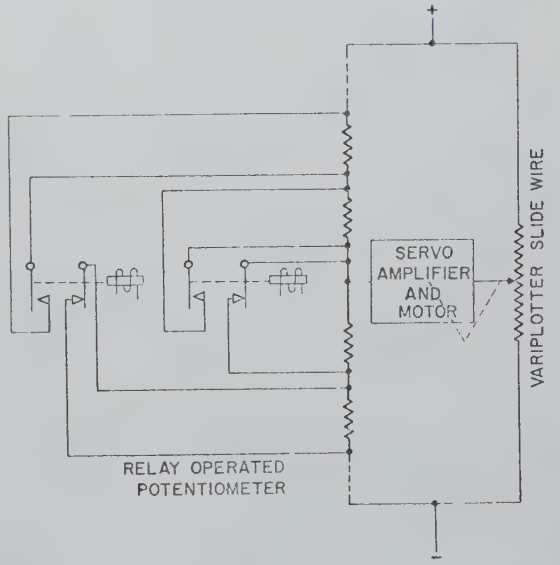

Fig. 7—Diagram of digital-to-analog converter and bridge circuit for automatic plotter.

Plotter has been designed to facilitate calibration and servicing. A series of switches insert preset calibration voltages into any variable. Neon indicator lights are provided on registers, and numbers may be manually inserted into buffer register. Plotting cycle may then be carried out step by step in order to locate troubles.

[4] Manufactured by Kellogg Switchboard and Supply Co., Chicago, Ill.

[5] Manufactured by Electronic Associates, Inc., Long Branch, N. J.

[6] M. B. Bain, "Precision digital-to-analog converter methods for graphical plotters," to be published in *Proc. NEC*, 1955.

Odd Binary Asynchronous Counters*

J. E. ROBERTSON†

Summary—This paper describes a general method for modifying conventional binary asynchronous counters such that the counting register advances by any desired odd integer for each received count. The pertinent design features of conventional additive and subtractive asynchronous counters are reviewed. Simplification of the design of a counter which advances by an odd integer is achieved through use of a set of alternately additive and subtractive subcounters. An example of the logical design of a counter which advances by 13 is presented.

Introduction

AN UNUSUAL type of counter described by Ware[1] and Brown[2] is used in binary asynchronous computers patterned after the Institute for Advanced Study computer. Such counters employ a pair of gating operations which are mutually exclusive timewise to advance the state of a set of "true" toggles by one unit. This paper describes a general method for modifying such counters so that the state of the set of "true" toggles is advanced by any desired odd integer by each pair of gating operations.

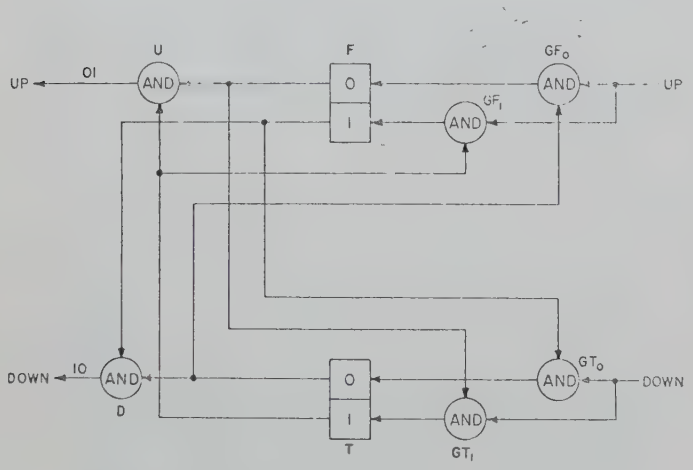

Fig. 1—Logical equivalent of one stage of an adding asynchronous binary counter.

Review of Counter Design Principles

One stage of the asynchronous counter[3] consists of a "true" toggle, a "false" toggle, circuits for gating the toggles to their allowed states, and circuits for forming a pair of gating levels to operate the next most significant stage. The logical equivalent of one stage of the asynchronous counter is shown in Fig. 1. The effect of the UP input gating operation is to set the false toggle F to agree with the true toggle T. For example, if $T=0$ *and* an UP input gating operation occurs, F is set to 0 by the "and" circuit GF_0. Similarly, the effect of the DOWN gating operation is to set the true toggle T to disagree with the false toggle F. The true and false toggles thus proceed through a Gray code sequence of states as alternate UP and DOWN input gating operations are applied (Table I). The UP and DOWN gating levels for the next most significant stage are formed by sensing the states 0 1 and 1 0, respectively, with the "and" circuits U and D. For a counter whose true toggles are to assume the sequence of states corresponding to the binary integers 0 to 2^{n-1}, n stages of the type illustrated by Fig. 1 are required. The process of counting in a two stage counter is indicated in Table II. It is

TABLE I
Sequence of States of True and False Toggles of One Stage

Input pulse	F	T
	1	0
up	0	0
down	0	1
up	1	1
down	1	0

TABLE II
Sequence of States of Toggles in a Two Stage Adding Asynchronous Counter

State of true toggles		Most significant stage		Least significant stage		Input gating operation
		F	T	F	T	
0	0	1	0	1	0	
				0	0	up
						down
0	1	0	0	0	1	
						up
				1	1	
						down
1	0	0	1	1	0	
						up
				0	0	
						down
1	1	1	1	0	1	
						up
				1	1	
						down
0	0	1	0	1	0	
						up
				0	0	

* Original manuscript received by the PGEC, August 18, 1955; revised manuscript received, November 10, 1955.

† Digital Computer Lab., Univ. of Illinois, Urbana, Ill.

[1] Willis Ware, "The logical principles of a new kind of binary counter," Proc. IRE, vol. 41, pp. 1429–1437; October, 1953.

[2] R. M. Brown, "Some notes on logical binary counters," Trans. IRE, vol. EC-4, no. 2, pp. 67–69; June, 1955.

[3] The asynchronous counters discussed here have been called "self-instructed counters" by Ware.

be noted that the sequence of states assumed by the true toggles is that of a conventional binary counter.

As has been pointed out by Ware and Brown, the adding asynchronous counter can be converted to a subtracting counter by interchanging the states used to form the UP and DOWN gating levels for the next most significant stage (Fig. 2). For this arrangement,

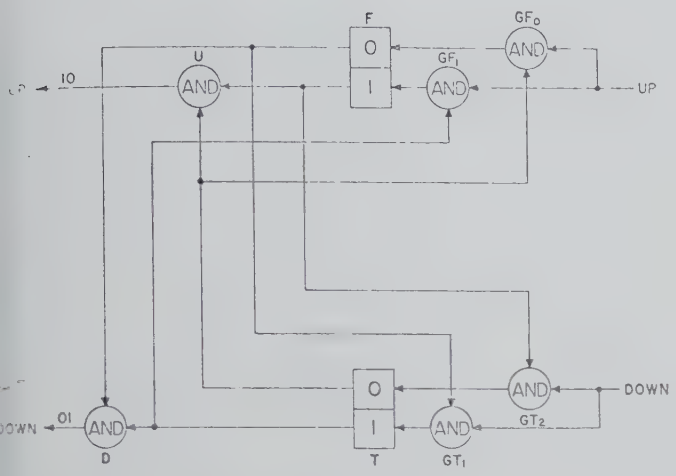

Fig. 2—Logical equivalent of one stage of a subtracting asynchronous binary counter.

the sequence of states is that shown in Table III, and the true toggles assume states corresponding to a descending sequence of binary integers.

TABLE III
SEQUENCE OF STATES OF TOGGLES IN A TWO-STAGE SUBTRACTING ASYNCHRONOUS COUNTER

State of true toggles		Most significant stage		Least significant stage		Input gating operation
		F	*T*	*F*	*T*	
0	0	0	0	1	0	up
				0	0	down
1	1	0	1	0	1	up
				1	1	down
1	0	1	1	1	0	up
				0	0	down
0	1	1	0	0	1	up
				1	1	down
0	0	0	0	1	0	up
				0	0	

Design of an Asynchronous Counter Which Advances by an Odd Integer

In some applications, it is desirable that an n-stage counter assume a sequence of states such that successive true states differ by an odd integer other than one. The counter designs described in the previous section can be easily modified for any specified odd integer q. The modification requires that the counter be subdivided into subcounters, with the subcounters alternately additive and subtractive.

For an n-stage counter, the stages are numbered 0, 1, 2, $\cdots$, $n-1$, where stage 0 is the least significant one. We then express q as an alternating series of powers of two. If q is in the range $-2^{n-1}<q<2^{n-1}$, then

$$q = \pm 2^{p_{k-1}} \cdots \mp 2^{p_3} \pm 2^{p_2} \mp 2^{p_1} \pm 2^{p_0}$$

with $0=p_0<p_1<p_2<p_3<\cdots<p_{k-1}<p_k=n$. The p_i are integers uniquely determined by the value of q. For example, if $q=13$, $q=+2^4-2^3+1=16-4+1$. The number of terms (k) in the series representation of q determines the number of subcounters. The sign of the term determines whether the corresponding subcounter is an adding or subtracting subcounter. The exponents p_i determine the number of stages in each subcounter. Specifically, sub-counter i ($i=0, 1, \cdots, k-1$) has $p_{i+1}-p_i$ stages numbered p_i, $p_i+1, \cdots, p_{i+1}-1$. If the sign of the term 2^{p_i} is positive, subcounter i is an adding subcounter; if the sign is negative, subcounter i is a subtracting one. For example, if $q=13$ and $n=5$, then $k=3$, and $p_0=0$, $p_1=2$, $p_2=4$. Three subcounters are:

Subcounter 0	stages 0 and 1	additive
Subcounter 1	stages 2 and 3	subtractive
Subcounter 2	stage 4	additive

The alternation of adding and subtracting subcounters simplifies the counting process when a carry (or borrow) is transmitted from one subcounter to the next most significant one. The input DOWN gating operation is applied to the least significant stage of each subcounter, except that it is inhibited by a carry (or borrow) from subcounter $i-1$. One requirement for the carry of an adding subcounter is that its true toggles are in the 1 state; similarly, a requirement for the borrow of a subtracting subcounter is that its true toggles are in the 0 state. The rules for inhibition of the UP gating operation require some elaboration. Suppose that subcounter i is an additive one and that all toggles of subcounter i are in the one state. Then the addition of a one to stage p_i should produce a carry whose effect is the addition of a one to stage p_{i+1}, the normal subtraction and the additive carry from stage p_i cancel one another; the net result is that we inhibit the UP gating operation, thereby preventing any change of the true toggle of stage p_{i+1}. In short, the conditions for a carry (or borrow) from a given subcounter are that all toggles are in the carry (or borrow) state and that an UP input is applied to its least significant stage. The effect of a carry (or borrow) from a given subcounter is to prevent an UP input from being applied to the next most significant subcounter. A block diagram of the counter is shown in Fig. 3.

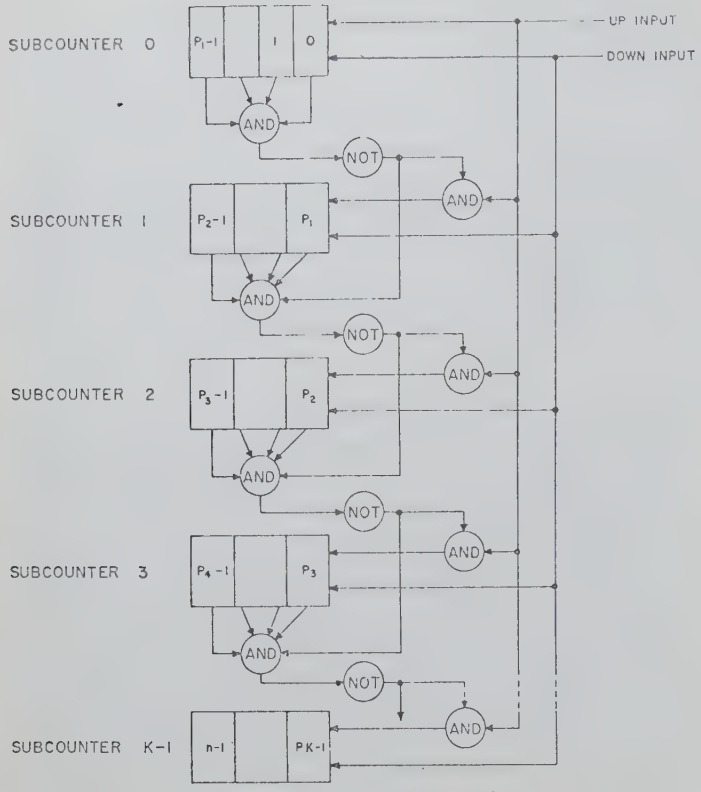

Fig. 3—Block diagram for an odd binary asynchronous counter.

The simplification achieved by use of the alternating series representation of q may be more apparent if we consider the design difficulties when the conventional positive series representation is employed (*e.g.* $q=13$, $=2^3+2^2+2^0$). Since all subcounters are additive, it is necessary when a carry arises in subcounter $i-1$ to initiate two counting operations at the least significant stage of subcounter i. Not only would the circuitry for generating an extra pair of gating operations be complicated, but additional time for the operations would be required as well.

Illustrative Example

The following example arose in connection with the design of a drum storage unit for the Illiac. It was desired that a set of 32 words comprising one track should be interlaced in such a way that for every fifth word, the count contained in the true toggles increased by 1. Inspection of Table IV reveals that an equivalent requirement is that the state of the true toggles should increase by 13 for each word. The equivalence may also be deduced from the fact that

$$5 \times 13 \equiv 1 \text{ modulo } 32.$$

As noted in the previous section $q=13$, $n=5$, $k=3$, $p_0=0$, $p_1=2$, $p_2=4$.

Three subcounters are required, as follows:

TABLE IV

Sequence of True States for Counter which Counts by 13's

0	0	0	0	0
0	1	1	0	1
1	1	0	1	0
0	0	1	1	1
1	0	1	0	0
0	0	0	0	1
0	1	1	1	0
1	1	0	1	1
0	1	0	0	0
1	0	1	0	1
0	0	0	1	0
0	1	1	1	1
1	1	1	0	0
0	1	0	0	1
1	0	1	1	0
0	0	0	1	1
1	0	0	0	0
1	1	1	0	1
0	1	0	1	0
1	0	1	1	1
0	0	1	0	0
1	0	0	0	1
1	1	1	1	0
0	1	0	1	1
1	1	0	0	0
0	0	1	0	1
1	0	0	1	0
1	1	1	1	1
0	1	1	0	0
1	1	0	0	1
0	0	1	1	0
1	0	0	1	1

Subcounter 0, additive, stages 0 and 1

Subcounter 1, subtractive, stages 2 and 3

Subcounter 2, additive, stage 4

The logical diagram of the desired counter which counts by 13's is shown in Fig. 4 (opposite). For the physical modification of an existing adding binary counter, the U and D "and" circuits (Figs. 1, 2) of stages 1 and 3 were used for forming the UP inputs to stages p_1 and p_2 (*i.e.*: 2 and 4), so that only $2\frac{1}{2}$ additional tubes were required for the modification. The approach initially considered involved use of a translation circuit requiring 15 tubes.

Conclusions

This paper presents a solution to a problem which was, to the author, somewhat difficult conceptually but simple in implementation. Although the description here applies specifically to asynchronous counters counting by odd integers, several extensions of the approach appear possible. An obvious extension is to counting by even integers. If an n-stage counter advancing by $2^r q$, with q an odd integer, is desired, it is sufficient to design a counter which advances by q in the $n-p$ most significant digits, with the p least significant digits always zero. It is thus possible to design a counter which advances by any integer, even or odd. It seems reasonable that the approach can also be employed in the design of other types of binary counters.

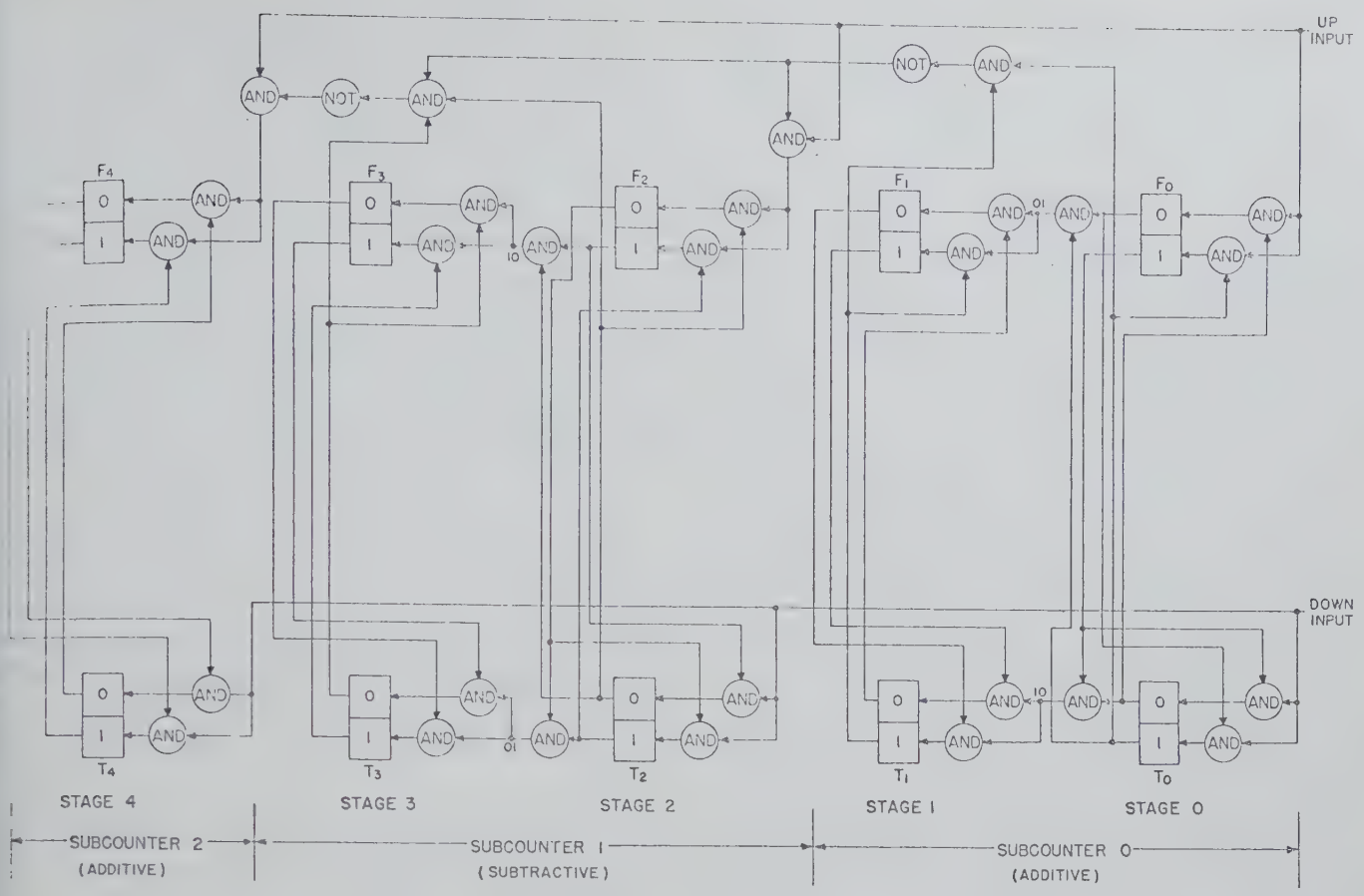

Fig. 4.—Logical diagram of counter which counts by 13's.

Complexity in Electronic Switching Circuits*

D. E. MULLER†

Summary—The complexity of an electronic switching circuit is defined in a sufficiently general way so that most definitions which are presently used may be included. If $\phi(p, q)$ is the complexity of a p input q output circuit which has been minimized then we may define $E(p, q)$ as the maximum of $\phi(p, q)$ over all p input, q output circuits. In spite of the generality of the definition of complexity one may obtain the following inequality which gives upper and lower bounds on this maximum complexity:

$$C_1 2^r/r \leqq E(p, q) \leqq C_2 2^r/r$$

where $r = p + \log_2 q$. In this expression C_1 and C_2 are constants independent of p and q which depend upon the definition of complexity. These theoretical bounds are compared with those obtained from a few known circuit designs.

Introduction

A QUALITATIVE appreciation of the complexity required of a circuit forming a given switching function has long existed. As switching circuits are designed, many alternative circuits may be imagined which perform the desired function but which have different properties of speed and economy. Such properties are dependent upon the type of switching elements used in the circuit. The relative importance of these properties to the designer depends upon the use to be made of the circuit. A general theory of complexity would seem to be impossible to construct because of the absence of any set criterion of complexity, yet we shall show here that in spite of this absence it will be possible to develop certain general results concerning complexity which apply to a broad class of criteria.

It is to be hoped that these results will be helpful to the circuit designer faced with the problem of designing exceedingly complex circuits with many inputs and outputs. In such cases an "order of magnitude" estimate of the complexity to be expected in the circuit may be useful as experience does not exist to guide one.

The situation is somewhat different if relays rather than electronic circuits are used as switching elements.

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A convenient measure of the complexity of a relay circuit having no secondaries may be taken as the number of relay contacts. Using this criterion and others, Shannon has made an analysis of the complexity required in the construction of two terminal switching functions.[1] In his analysis of a general two-terminal network no restriction was made that the circuit be of the series-parallel type. Although the results of Shannon concerning relay switching circuits in no way overlap the theorems in the present exposition concerning electronic switching, it may be seen that a similarity exists between the fundamental properties of the two types of circuits.

Definition of Complexity

Electronic switching circuits are constructed from certain types of elements which perform basic logical operations. Typical types are the familiar "and," "or," and "not" circuits. We shall imagine a set of such element types which may be combined to form any given switching function. This set, which we shall call a basic set, will be used to construct all switching circuits. Each element type will be taken as having a finite number of imputs and one output. Let the element types be numbered $1, 2, \cdots, n$ and to each type let a numerical value be assigned $a_1, a_2, \cdots, a_n$. The value or complexity of a circuit composed of such elements will be defined as the sum of the values of the individual elements of which it is formed.

This definition of complexity is general insofar as it permits an arbitrary choice of the members of the basic set of decision elements and values to be attached to them. It does not, however, allow one to treat directly circuits including non-logical elements, nor does it permit the consideration of other economies such as economies in time or physical arrangement.

Given a basic set of elements $1, 2, \cdots, n$ with values $a_1, a_2, \cdots a_n$ where $a_i > 0$ for each $i = 1, 2, \cdots, n$, we may form only a finite number of circuits having value less than or equal to some fixed number M. To prove this result we note that only a finite number of element types exists in the basic set itself and consequently only a finite number of combinations of elements may be chosen whose total value is less than or equal to M. Each such combination may be interconnected in only a finite number of ways and thus the total number of circuits is finite.

The action of a general combinational circuit having p inputs $x_1, x_2, \cdots, x_p$ and q outputs $y_1, y_2, \cdots, y_q$ may be completely described by specifying each output as a Boolean function of the inputs

$$y_i = y_i(x_1, x_2, \cdots, x_p) \qquad i = 1, 2, \cdots, q.$$

Let us also assume that the constant inputs 0 and 1 are available when constructing these functions.

[1] C. E. Shannon, "The synthesis of two-terminal switching circuits," *Bell Sys. Tech. Jour.*, vol. 28, pp. 59–98; January, 1949.

By hypothesis each of these functions may be constructed from the basic set of decision elements so that, alternatively, given a set of functions it is possible to form a circuit having outputs corresponding to them. Let this circuit have some value V. Of the circuits equivalent in action to this one only a finite number have value less than or equal to V. The minimum value among this set of circuits we shall call $\phi(y_1, y_2, \cdots, y_q)$. It is a numerical function of the q Boolean functions y_i and represents the minimum value for which the given circuit may be constructed. While the function ϕ exists for any set of Boolean functions y_i we note that it will depend upon the basic set of decision element types used and upon the values attached to these types.

Generality of the Theory

One might feel that any theory of the ϕ function would be extremely specialized since it depends so strongly upon the basic set. The first theorem shows, however, that to a constant multiplying factor its behavior is independent of the basic set which is used. We may proceed, therefore, to study the behavior of ϕ with increasing p and q up to a constant multiplying factor.

Theorem 1: Two basic sets of decision elements, set 1, and set 2, have m and n element types respectively with values $a_1, a_2, \cdots, a_m$ and $b_1, b_2, \cdots, b_n$. If ϕ_1 is the minimal value of a circuit with outputs $y_1, y_2, \cdots, y_q$ using elements from set 1, and ϕ_2 is the minimal value using elements from set 2, then there exist constants K_1 and K_2 such that

$$K_1\phi_1 \leqq \phi_2 \leqq K_2\phi_1. \tag{1}$$

The constants K_1 and K_2 depend only upon the basic sets and their values and not upon the functions y_i.

Proof: Since ϕ_1 represents the minimal value for constructing the q output functions y_i from elements of set 1, and since only a finite number of circuits have values less than some fixed V, we may actually realize a circuit having value ϕ_1 formed from set 1 elements and producing the y_i. Now since any Boolean function may be formed by combining elements of set 2, we may construct each one of the m element types in set 1 from set 2 elements alone. Let the values of these circuits as formed from set 2 elements be $a_1', a_2', \cdots, a_m'$. If in the q output circuit referred to above we replace each set 1 element by its circuit formed from set 2 elements we may expect the value of the circuit to change but its action to remain unchanged. Let the value of the new circuit be W. Clearly $W \geqq \phi_2$ since ϕ_2 is the minimal value for such a circuit composed of set 2 elements. On the other hand

$$W/\phi_1 \leqq \max\,(a_1'/a_1, a_2'/a_2 \cdots a_m'/a_m) = K_2$$

since each replacement of the ith set 1 element by a circuit composed of set 2 elements will change the effective value of that element by the factor a_i'/a_i.

ce the value of the entire circuit may never exceed . Combining our two results we obtain $\phi_2 \leqq W \phi_1$, which is the right-hand side of (1). To obtain the -hand side of this inequality we may reverse the of set 1 and set 2 in the above argument. A new nstant, which may be called $1/K_1$, will be obtained ving the property $\phi_1 \leqq (1/K_1)\phi_2$ which is equivalent the left-hand side of (1).

An interesting analogy to this theorem exists in the heory of translation of languages. One may regard ϕ_1 the length of a message ideally expressed in the first anguage (say English) and ϕ_2 as the length of the same message ideally expressed in the second language (say French). The same type of argument as in the above proof may be used to establish inequality (1). We may begin by defining $a_1, a_2, \cdots, a_m$ as the lengths of words in English. Then $a_1', a_2', \cdots, a_m'$ would correspond to the lengths of their definitions in French. Since the most inept translation from English to French would consist of replacing each English word by its French definition we are able to set an upper bound on the length of the ideal French expression ϕ_2 if we know the length of the ideal English expression ϕ_1. It is not surprising that this analogy exists between languages and switching circuits since one may regard a switching circuit as a way of describing a set of Boolean functions.

We now wish to study the behavior of the function up to a multiplying constant as p and q are allowed to increase. Since this function depends upon the Boolean functions y_i it will be a rather inconvenient one to study so we consider instead a new function $E(p, q)$. The function, $E(p, q)$, is defined as the maximum of the ϕ functions for circuits having p inputs and q outputs. Thus any circuit with p inputs and q outputs may be constructed from circuits having value E or less and yet there is at least one circuit which requires value E for its construction. This satisfies a theorem similar to Theorem 1 which may be proved directly from it.

Theorem 2: Two basic sets of decision elements, set 1 and set 2, have E-functions as defined above which are E_1 and E_2. These functions are related by

$$K_1 E_1(p, q) \leqq E_2(p, q) \leqq K_2 E_1(p, q) \tag{2}$$

where K_1 and K_2 are defined as in Theorem 1 and hence are independent of p and q.

Proof: There is at least one set of functions $y_1, y_2, \cdots, y_q$ having the property that $\phi_2(y_1, y_2, \cdots, y_q) = E_2(p, q)$, since E_2 is the maximum of all such functions ϕ_2 and they are finite in number. Also we see that $\phi_1(y_1, y_2, \cdots, y_q) \leqq E_1(p, q)$ since $E_1(p, q)$ is the maximum of all ϕ_1 so that

$$E_2(p, q) = \phi_2 \leqq K_2 \phi_1 \leqq K_2 E_1.$$

The left-hand side may be obtained by a like argument.

Comparisons of Numerical Estimates

A numerical estimate of the maximum complexity is obtained in the next theorem. Theorems 1 and 2 make this estimate meaningful since they show that numerical bounds do exist in all cases for the function $E(p, q)$.

Theorem 3: The function $E(p, q)$ is bounded by

$$C_1 2^r/r \leqq E(p, q) \leqq C_2 2^r/r \tag{3}$$

where $r = p + \log_2 q$ and the constants C_1 and C_2 depend only on the basic set of decision elements used and the values attached to these elements, and are independent of p and q. The integers p and q must satisfy the relationship $1 \leqq q \leqq 2^{2^p}$.

Since the proof of this theorem is rather lengthy it is presented as an appendix. The theorem provides universal bounds on the complexity of a circuit which are valid regardless of the number of inputs and outputs. Inequality (3) would be most useful if one could use it to estimate the complexity to be expected in circuits having large numbers of inputs and outputs when one has only had experience with much simpler circuits. The complexity would be taken as roughly proportional to $2^r/r$ and an estimate could thus be made. Whether or not such an estimate is valid depends upon the relative magnitudes of the constants C_1 and C_2. If their ratio is close to unity the estimate would be good, while if not, one might learn little from it. Since the theorem itself does not specify the relative magnitudes of C_1 and C_2, we must attempt to compare the $2^r/r$ rule with known complexities.

A particular set of decision elements and values is used in the Harvard publication "Synthesis of Electronic Computing and Control Circuits."[2] An extensive analysis of complexities for all circuits having up through four inputs and one output was made by the authors using their set of decision elements. The most complex circuits with two, three, and four inputs had complexities 4, 9, and 20 respectively. Since $r = p$ when one output exists we may compare the relative magnitudes of these numbers with $2^2/2 = 2$, $2^3/3 = 8/3$, and $2^4/4 = 4$ which one obtains by use of the formula. Although the comparison is not particularly encouraging it should serve for order of magnitude estimates which do not exist at present when the number of inputs exceeds seven or eight.

Earlier analyses of this sort have never yielded similar formulas for both upper and lower bounds as in (3). J. T. Culbertson[3] obtains the equivalent of $C_2 2^p$ for the right-hand bound and $C_1 2^{p/2}$ for the left-hand bound in (3). When one output is involved and $p = r$ we obtain much wider bounds when Culbertson's formulas are used and p is large than using the present formulas. Serrel[4] obtains the even higher upper bound of $p2^p$ and does not find a lower bound.

[2] "Synthesis of Electronic Computing and Control Circuits," Staff of the Computation Lab., Harvard Univ. Press, Cambridge, Mass.; 1951.

[3] J. T. Culbertson, "Even in memoryless robots there is no small number of central cells sufficient for all input-output Specifications," unpublished report, Rand Corp.; August 12, 1952.

[4] R. Serrell, "Elements of Boolean algebra for the study of information handling systems," Proc. IRE, vol. 41, pp. 1366–1379; October, 1953.

Conclusion

By way of conclusion we may say that a rather rough method has been found for estimating the maximum complexity of electronic switching circuits similar to that discovered by Shannon[1] in the case of relay switching circuits. Such an estimate is likely to be useful in the design of circuits having many inputs and outputs. Another use may appear in the evaluation of the relative merits of various systematic processes of circuit simplification such as the Harvard Chart method[2] and others.[5]

Appendix

Proof of Theorem 3: Separate treatments must be made of the right and left-hand sides of (3). To prove the right-hand inequality it is sufficient to exhibit a circuit of value $\leqq C_2 2^r/r$ having the q outputs $y_1, y_2, \cdots, y_q$ for any set of such Boolean functions. In view of Theorem 2 we may construct this circuit using any basic set we choose since any constant factor may be absorbed in C_2.

In the circuit to be formed we shall employ a basic set consisting of a single type of decision element. This element has three inputs, one output, and represents in its action the Boolean function $ab + \bar{a}c$ where a, b, and c are the three inputs. We shall begin by forming all possible Boolean functions of the first k of the p inputs. Any function of k inputs may be constructed using a single element of the type described above provided all functions of the first $k-1$ of the k inputs are available. This result follows from the formula.

$$f(x_1, x_2, \cdots, x_k) = x_k f(x_1, x_2, \cdots, x_{k-1}, 1) + \bar{x}_k f(x_1, x_2, \cdots, x_{k-1}, 0). \quad (4)$$

Thus if all functions of k variables are to be constructed the number of elements need not exceed the number of functions. This number is 2^{2^k}. Use may be made of these functions in the construction of the q output functions y_i. Each output function y_i may be formed from two $p-1$ input functions by use of (4). By repeated application of (4) we may therefore form each y_i from 2^{p-k} of the k input functions and $2^{p-k}-1$ of the elements used above. If each of the q outputs is formed separately in this way the total number of elements required is

$$N = 2^{2^k} + q2^{p-k} - q. \quad (5)$$

Since the choice of k has not been fixed we may adjust k so that N is small. Although a formal minimization leads to a transcendental equation we may accomplish our purpose by choosing an approximate minimum which yields $N < C_2 2^r/r$ for some constant C_2. Interestingly enough, a similar expression was encountered by Shannon in his treatment of relay switching circuits.[1] His object, however, was to obtain an asymptotic value rather than an upper bound. An arbitrary choice of k for which $N < C_2 2^r/r$ is satisfied is given by

$$\log_2 (r - \log_2 r) - 1 \leqq k < \log_2 (r - \log_2 r). \quad (6)$$

Since k must remain an integer we can uniquely define k by (6). Now N is a function of k having positive second derivative [by (5)], so that the larger value of N at the two limits of (6) will represent an upper bound for N. At the right-hand limit

$$N = \frac{2^r}{r} + \frac{2^r}{r - \log_2 r} - q < 3\frac{2^r}{r},$$

while at the left hand limit

$$N = \left(\frac{2^r}{r}\right)^{1/2} + \frac{2^{r+1}}{r - \log_2 r} - q < 5\frac{2^r}{r}.$$

Thus a method of construction is obtained which yields the right-hand limit of (3) whenever $k \leqq p$, that is to say whenever $\log_2 (r - \log_2 r) \leqq p$. If this condition is not satisfied, however, we may take $k = p < \log_2 (r - \log_2 r)$ and obtain

$$N = 2^{2^k} = 2^{2^p} < 2^{2^{\log_2 (r - \log_2 r)}} = \frac{2^r}{r}.$$

Therefore we obtain the right-hand limit for all $q \geqq 1$.

A different method must be used to obtain the lower limit of (3). A numerical estimate of the number L of different circuits which may be constructed with complexity M or less may be obtained. This number must be greater than the number K of p input q output functions which may be formed. For this latter number we have

$$K = 2^{q2^p}$$

since each of the q outputs $y_1, y_2, \cdots, y_q$ may be any one of the 2^{2^p} possible Boolean functions of p variables.

If decision elements of the type which were used in the first part of the proof are used again, we may take M as the number of such elements. $p+2$ signals are available as inputs; they are $x_1, x_2, \cdots, x_p$, 0, 1, and M signals are available from the decision elements. Therefore to each of the $3M$ decision element inputs and to each of the q outputs from the circuit we may connect any one of the $M+p+2$ signals giving

$$L \leqq (M + p + 2)^{3M+q}.$$

This figure would be reduced somewhat if account were taken of possible permutations among the decision elements and permutations among the lines going to a single element. Such refinements will not be necessary for the proof of Theorem 3. We now seek a lower bound M_L for M. Any M_L satisfying

$$(M_L + p + 2)^{3M_L+q} < 2^{q2^p} \quad (7)$$

will be a lower bound for M since if M were as small as M_L we could no longer have $K \leqq L$ (that is to say not enough circuit configurations are possible to produce the variety of output functions required). If we let

[5] D. E. Muller, "Application of Boolean algebra to switching circuits design and error detection," Trans. IRE, vol. EC-3, pp. 6–12; September, 1954.

$C_1 2^r/r$ and take the logarithm to the base 2 of both sides of (7) we find that the inequality becomes

$$(3C_1 2^r/r + q) \log_2 (C_1 2^r/r + p + 2) < 2^r. \quad (8)$$

This inequality must be proved for some value of C_1 and all r if we are to obtain the left side of (3). We begin by noting that if $q \geqq C_1 2^r/r + p + 2$ then $M_L = C_1 2^r/r$ is indeed a lower bound since fewer distinct signals than outputs are present. Thus circuits having q distinct outputs cannot be constructed if $M = M_L$. Since 2^{2^p} distinct functions may be formed we have $M_L = C_1 2^r/r$ as a lower bound whenever

$$C_1 2^r/r + p + 2 \leqq q \leqq 2^{2^p}.$$

In the range

$$1 \leqq q \leqq C_1 2^r/r + p + 2$$

we have

$$(3C_1 2^r/r + q) \log_2 (C_1 2^r/r + p + 2) \leqq (4C_1 2^r/r + p + 2) \log_2 (C_1 2^r/r + p + 2).$$

Now $C_1 2^r/r \geqq p + 2$ if $r \geqq p$ is made large enough.

$$(4C_1 2^r/r + p + 2) \log_2 (C_1 2^r/r + p + 2) \leqq 5C_1 2^r/r \log_2 2C_1 2^r/r.$$

If we make $C_1 = 1/5$ we obtain

$$5C_1 2^r/r \log_2 2C_1 2^r/r = 2^r/r(r - \log_2 r + \log_2 2/5) \leqq 2^r$$

thus proving (8) for sufficiently large r. Since only a finite number of cases exist with r less than any given amount we may always take C_1 small enough to cover these cases. Thus the inequalities of (3) are proved using a special type of decision element. Theorem 2, however, allows us to generalize to the use of any basic set of decision elements provided we change the constants C_1 and C_2 accordingly. Since the constants of Theorem 2 depend upon the arbitrary values placed upon the members of the basic set it would seem to be impossible to narrow the inequalities (3) further without specializing to a particular basic set. If an assumption of no feedback is used in the calculation of L it is possible to lower its bound somewhat but the limiting value of M_L remains the same and the more involved analysis is of no advantage.

On the Wiring of Two-Dimensional Multiple-Coincidence Magnetic Memories*

N. M. BLACHMAN†

Summary—The application of Minnick and Ashenhurst's technique of p-fold multiple-coincidence magnetic storage in an $n \times n$ array of cores is shown to require finding $(p-2)$ orthogonal Latin squares of order n. The value of this technique lies in the reduction it effects in the disturbance of unselected cores. A method is suggested for reducing this disturbance to a level lower than that obtained by Minnick and Ashenhurst, by the application of reverse currents to the unselected interrogating wires during interrogation. The disturbance of unselected cores can be reduced to zero if $p = n+1$. In this case, $(n+1)$ cores can be added to the store at the expense of a single additional interrogating wire. The resulting array of cores and interrogating wires is closely related to the finite projective geometry of order n.

Introduction

THE MULTIPLE-COINCIDENCE magnetic storage technique recently proposed by Minnick and Ashenhurst[1] will be shown to require, in effect, the finding of a set of orthogonal Latin squares, and an interesting though impractical extension of this technique will be shown to imply the threading of magnetic cores along the lines of a finite projective geometry. Minnick and Ashenhurst's technique involves threading a magnetic-core matrix memory nxn with p sets of interrogating wires $(p > 2)$ in order to reduce the disturbance of uninterrogated cores. It is required that p wires, one from each set, thread each core, and that no other core be threaded by more than one of the set of p wires threading a given core. In this way, it is possible to keep the disturbance of uninterrogated cores down to $1/p$ of the full interrogating current.

In particular, Minnick and Ashenhurst have suggested threading the matrix of cores with p sets of n interrogating wires in such a way that 1) each wire threads n cores, 2) no core is threaded by two wires in the same set, 3) any two wires not in the same set thread exactly one core in common, and 4) one set of n wires threads (or defines) the columns of the matrix and another set the rows, in the manner that is usual

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[1] R. C. Minnick and R. L. Ashenhurst, "Multiple coincidence magnetic storage systems," *J. Appl. Phys.*, vol. 26, p. 575; 1955.

for coincident-current magnetic storage. By comparing 1) with 4) with the definition of orthogonal Latin squares, which follows, it can be seen that the remaining sets of wires must thread the array in a manner describable by $(p-2)$ mutually orthogonal Latin squares of order n.

Orthogonal Latin Squares

A Latin square of order n consists of n symbols, each repeated n times, arranged in an $n \times n$ array in such a way that no symbol appears twice in the same row or the same column. Two Latin squares are said to be orthogonal if, when they are superposed, each (ordered) symbol pair occurs once and only once. If we regard the n symbols appearing in each of $(p-2)$ orthogonal Latin squares as representing the n wires of one of the sets of interrogating wires, and if we suppose that our n^2 cores are arranged in an $n \times n$ array, each one threaded by the wires whose symbols occur in the corresponding position in any of the $(p-2)$ Latin squares, as well as by a wire of each of the two sets mentioned in 4), threading rows and columns, we see that 1)–4) define a set of $(p-2)$ mutually orthogonal Latin squares.

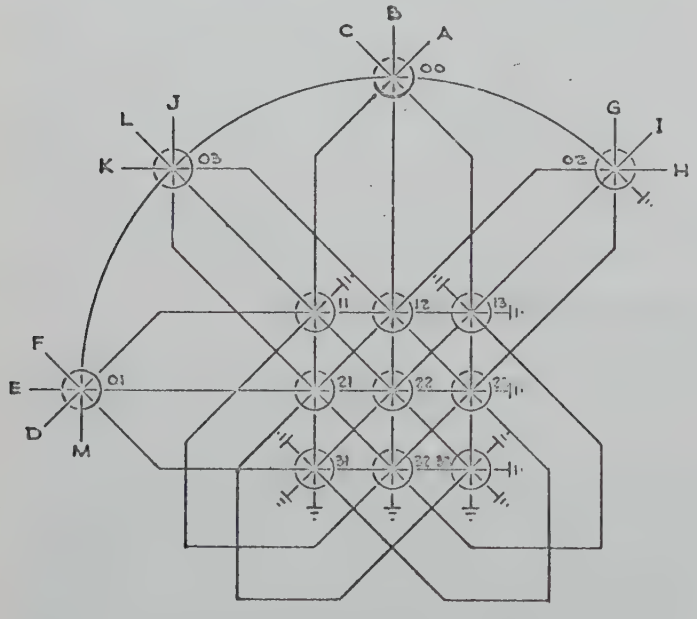

Fig. 1—Plane projective geometry of order $n=3$ based on the two orthogonal Latin squares $\begin{matrix} HGI & JKL \\ HIG & LJK \\ IGH & KLJ \end{matrix}$, showing how 13 cores (00-33) may be threaded by 13 interrogating wires (A-M) with each wire threading 4 cores and 4 wires threading each core.

Fig. 1 without cores 00, 01, 02, and 03 and wire M would illustrate the case of $n=3$. Table I illustrates the case of $n=4$ (disregard the fifth line of the Table for the present); (c)–(e) are three orthogonal Latin squares of order $n=4$, and (a) and (b) represent the usual wiring of the rows and columns of the array of cores. If we were to take $p=5$ and make use of all three Latin squares as well as (a) and (b), the top left-hand core, for example, would be threaded by interrogating wires A, E, I, M, and Q. The wires I and L would thread the diagonals of the array. Superposing (c) and (d), we see that, because of their orthogonality, the pair LP, for example, occurs only once, in the top right position; *i.e.*, the interrogating wires L and P, of different sets, thread only the top right-hand core in common.

Thus, the application of Minnick and Ashenhurst's technique fundamentally requires threading the array of n^2 cores according to $(p-2)$ orthogonal Latin squares of order n rather than according to their more restrictive finite analytic geometry, which is adequate for $n=3$, $p=3$ or 4, but not for $n=4$, $p>3$. However, the circuitry required to select the proper interrogating wires for a given core may become unwieldy for $p>3$, so that a single Latin square $(p=3)$, which is readily found for any n by Minnick and Ashenhurst's geometry, may be all that can be put to practical use.

TABLE I
Wiring of Array of Order $n=4$

(a)	(b)	(c)	(d)	(e)
AAAA	EFGH	IJKL	MNOP	QRST
BBBB	EFGH	JILK	OPMN	TSRQ
CCCC	EFGH	KLIJ	PONM	RQTS
DDDD	EFGH	LKJI	NMPO	STQR
AEIMQ	BFJNR	CGKOS	DHLPT	UUUUU

Reverse Current in Unselected Wires

With p sets of interrogating wires, an interrogating current of only I/p is required in each of the p wires threading the selected core, resulting in a disturbance of I/p in the unselected cores threaded by these wires. By passing a reverse current of $I/p(2p-1)$ through all unselected interrogating wires at the time of interrogation, in the manner suggested for the case $p=2$ by Rajchman,[2] it is possible to reduce the maximum disturbance of unselected cores to $I/(2p-1)$.

If $p=n+1$, each of the $(n+1)$ interrogating wires threading a selected core threads $(n-1)$ unselected cores, which, according to 3), are all distinct; *i.e.*, the selected interrogating wires thread $(n+1)(n-1)=n^2-1$ cores in all. Thus, every unselected core is threaded by one selected interrogating wire. By passing a reverse current of $I/n(n+1)$ through every unselected wire at the time of interrogation, it is then possible to reduce to zero the disturbance of the unselected cores.

If we were to take $p>n+1$, the p interrogating wires threading a selected core would each have to thread $(n-1)$ distinct unselected cores—$p(n-1)$ in all—and we would reach a contradiction, since there are only (n^2-1) unselected cores. Thus, there can be at most only $(n-1)$ orthogonal Latin squares of order n. A set of $(n-1)$ orthogonal Latin squares of order n is known as a "complete set." A complete set exists for n equal to any power of a prime.[3] Little is known about the

[2] J. J. Rajchman, "Static magnetic matrix memory and switching circuits," *RCA Review*, vol. 13, p. 183; 1952.
[3] H. B. Mann, "Analysis and Design of Experiments," Dover Publications, New York, pp. 87–106, 1949.

other cases except $n=6$; it has been shown that there are not two orthogonal Latin squares of order 6.

Finite Projective Geometry

The system with $p=n+1$, which requires $(n+1)n$ wires for n^2 cores (Minnick and Ashenhurst illustrated the case $n=5$, $p=6$, where 25 cores are threaded with 30 interrogating wires), has an interesting extension; $(n+1)$ cores can be added to the array with the inclusion of a single additional interrogating wire. All of the wires of each of the $p=n+1$ sets are threaded through one of the additional cores, and the additional interrogating wire is threaded through all of the additional cores. This is illustrated in Table I for $n=4$; the additional 5 cores take the 5 positions along the bottom of the array, and the additional interrogating wire is called U. The core at the right-hand end of the bottom line, for example, is threaded by wires Q, R, S, T, and U.

Under this type of extension of the multiple-coincidence system with $p=n+1$, there is one and only one interrogating wire that passes through any distinct pair of cores, and there is one and only one core common to any distinct pair of wires. Each wire threads $(n+1)$ cores, and each core is threaded by $(n+1)$ wires. There are (n^2+n+1) cores altogether, and an equal number of wires. Regarding the cores as points and the wires as lines, we have what is known as the finite plane projective geometry of order n, whose existence is closely tied up with the existence of a complete set of orthogonal Latin squares of order n. All of the points and all of the lines in this geometry have the same topological properties.[4] Fig. 1 illustrates the case $n=3$.

With an array of (n^2+n+1) cores threaded with (n^2+n+1) interrogating wires along the lines of a finite plane projective geometry of order n, the interrogating wires are no longer divisible into p sets of n wires. Nevertheless, the $p=n+1$ wires threading any selected core still thread every unselected core once, and the application of a reverse current of $I/n(n+1)$ to all unselected wires at the time of interrogation, therefore, still reduces to zero the disturbance of the unselected cores. No advantage is obtained with this $p=n+1$ system over a memory having (n^2+n+1) interrogating wires, each threading a single core. However, if a sufficiently simple method can be devised for selecting the appropriate p wires to interrogate any given core $(p<n+1)$, one of the foregoing memory systems may be found to be advantageous. An investigation of multiple-coincidence magnetic storage of higher dimensionality might also prove fruitful.

[4] F. W. Levi, "Finite Geometrical Systems," Univ. of Calcutta, 1942.

A Programmed Variable-Rate Counter for Generating the Sine Function*

J. N. HARRIS†

Summary—**The sine curve is approximated by a set of straight line segments whose slopes are chosen to be integral multiples of a binary fraction. A programmed counter counts up or down at a rate proportional to the slope, thus generating an approximate sine function. Using (360/256)≈1.4 degree intervals and four integral slopes, ±0(1/128), ±1(1/128), ±2(1/128), ±3(1/128), the maximum difference between the true and the generated value is 0.014 and occurs at 36.6 degrees. The extension of this method to higher accuracy and to other functions is indicated.**

Introduction

THE function sin θ may be approximated with surprising accuracy with only a few straight line segments. If the slope of each of these line segments is chosen so as to be an integral multiple of a binary fraction, it is possible to use a programmed counter whose rate of counting is proportional to the slope of the line segments and hence, approximate the sine function.

A counter based on this principle has been designed which will generate, at 1.4° intervals, the successive values of the sine of a continuously increasing angle; *e.g.*, a rotating shaft.

Line Segments

Fig. 1 shows how sin θ is approximated by a series of straight line segments. The slope, m, of each segment is given in units of (1/128). Four integral values are required, viz., $\pm 0(1/128)$, $\pm 1(1/128)$, $\pm 2(1/128)$ and $\pm 3(128)$. Fig. 2 gives a detailed view of this approximation for the first quadrant. The difference between sin θ and the approximation, $\overline{\sin \theta}$, is shown in Fig. 3.

The positions of the straight lines were determined graphically by the "cut and try" process. In order to

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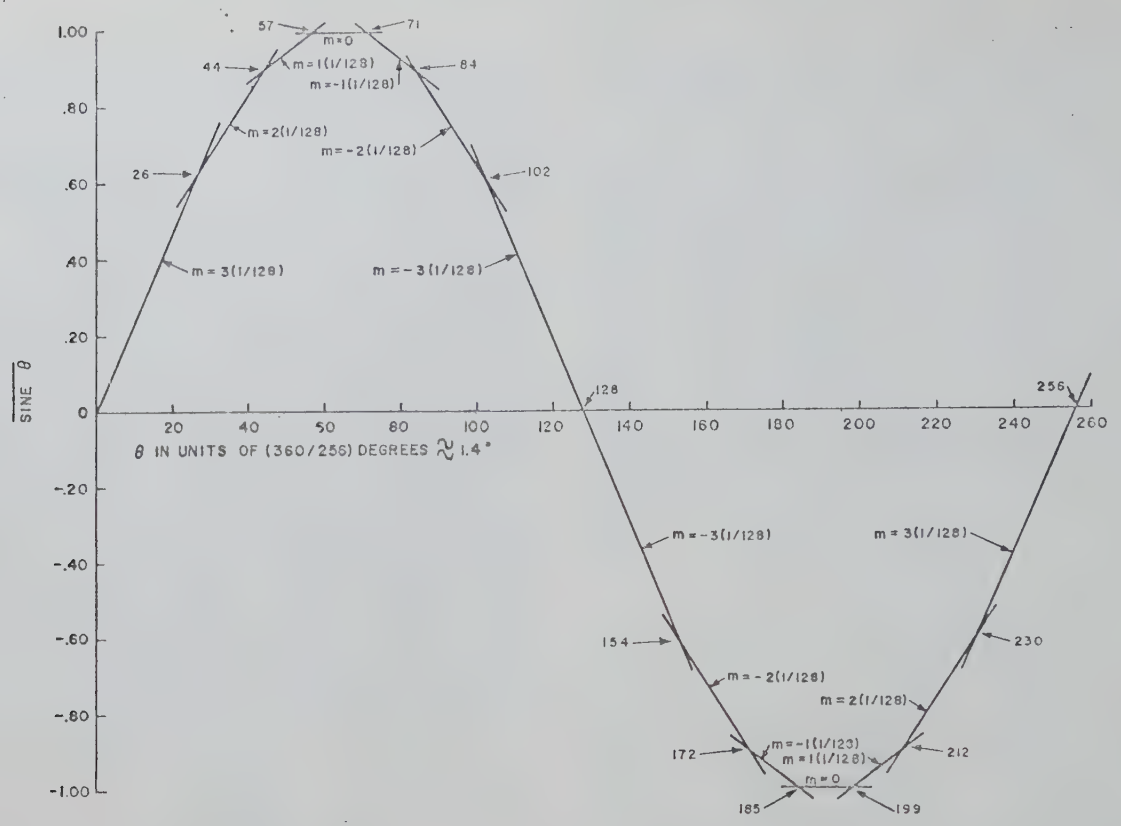

Fig. 1—Graph of $\overline{\sin \theta}$ (counter representation of $\sin \theta$) with slopes and positions of change in slope indicated.

cover the greatest portion of the curve with a single line, the lines were allowed to cut through the curve, instead of being tangent to it, thus giving + and − errors in the approximation. The lines were shifted until the error arising from this approximation was at a minimum. The approximate location of the maximum error was apparent from the graph, the exact value being determined by calculation for several points near this location.

Variables

In the following analysis, bit-positions will be represented by capital letters with subscripts as, A_i, where $i=1$ for the least significant position.

Since the θ increment is 360°/256, an 8-bit control counter, $A_8, A_6, \cdots A_1$, will be required. A 7-bit sine counter, $S_7, S_6, \cdots S_1$, will be used plus one sign bit, P. In addition, a slope counter B_2 and B_1 with the sign of

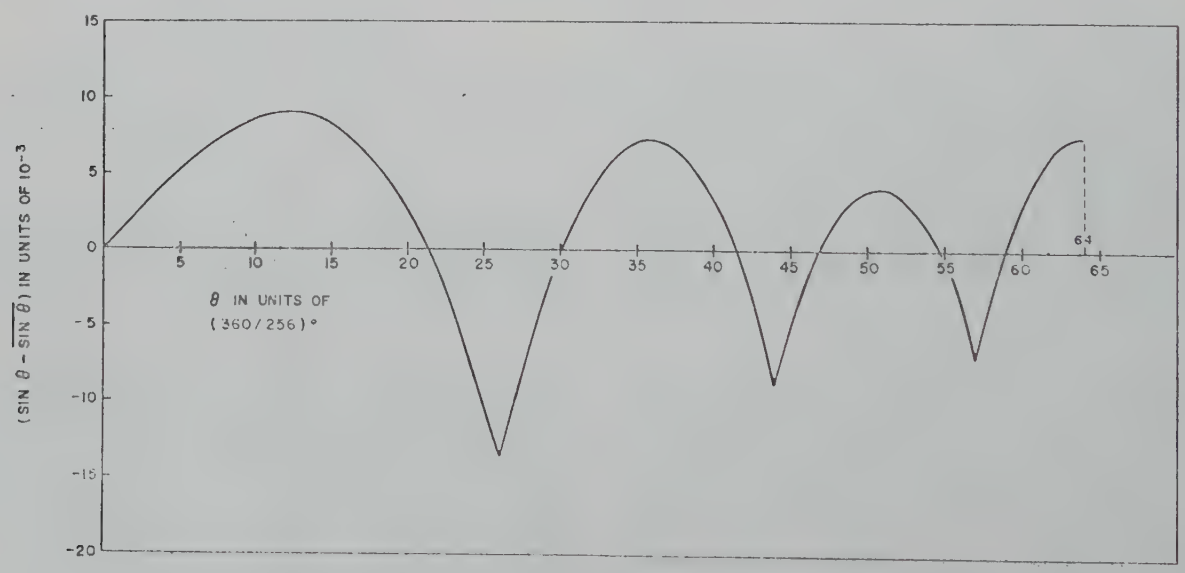

Fig. 2—Graph showing the smoothed differences between $\sin \theta$ and $\overline{\sin \theta}$ (counter).

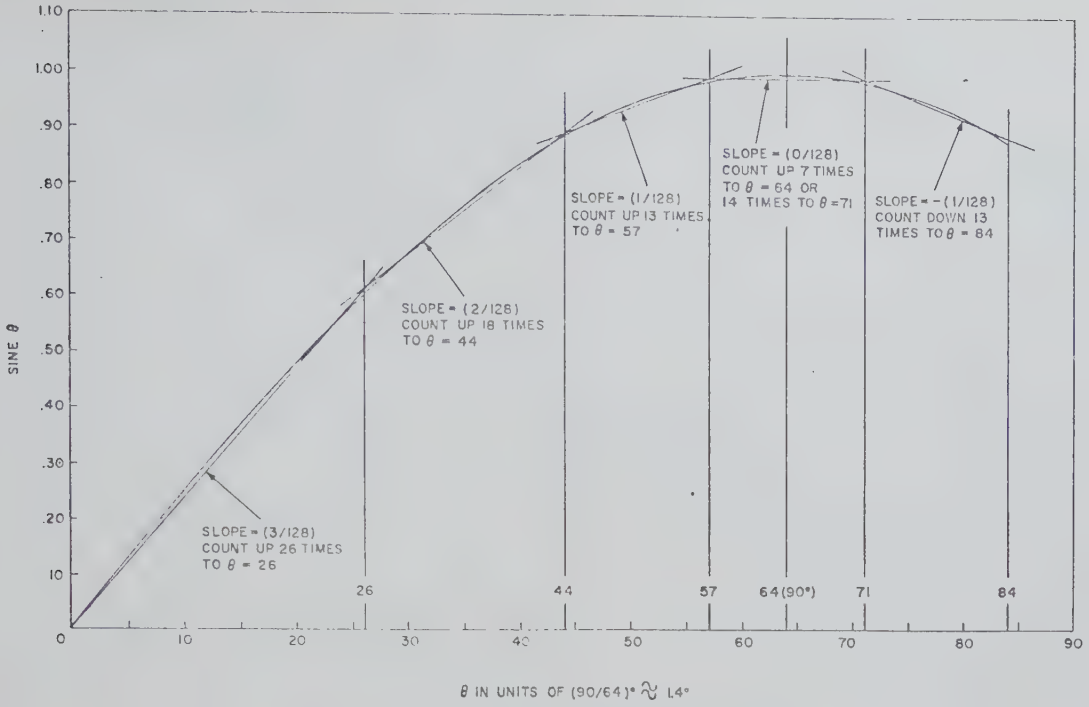

Fig. 3—Graph showing both $\sin\theta$ and $\overline{\sin\theta}$ (counter).

the slope, C, will be needed. These functions are tabulated for one quadrant in Table I on the following page. The negative values of $\sin\theta$ are formed by complementing each bit in turn and adding one. Positive values of the sine are represented by $P=\bar{0}$ and negative values of the sine by $P=\bar{1}$. Similarly, $C=0$ is a positive slope and $C=1$ is a negative slope.

Boolean Analysis

Use will be made of change equations[1,2] in the following Boolean analysis. A change in a variable, F (from one clock time to the next) from a 1 to a 0 is indicated by $\Delta_- F$, while a change from 0 to 1 is indicated by $\Delta_+ F$. Evidently the total change equation becomes the sum of these two changes of $\Delta F=\Delta_+ F+\Delta_- F$. We will assume that all counters start from a reset or zero condition.

Table I gives the values of the various functions for the first quadrant, the other quadrants being derivable from this table as indicated in Fig. 1.

Table II indicates all changes which occur in B_1, B_2 and C as the angle θ increases from 0° to 360°. (Refer to Table I and Fig. 1.) The changes in B_1 or B_2 (the slope counter) occur during the last count on the previous slope. Hence, the value of θ at this time is always one θ-unit less than the value at which the change actually occurs and which is shown in Fig. 1.

[1] J. S. Reed, M.I.T., "Symbolic design of digital computers," Lincoln Lab. memo (not generally available).
[2] J. S. Reed, "Symbolic synthesis of digital computers," Proc. of the Assn. for Computing Machinery, meeting at Toronto, Ont., p. 90, September 8–10, 1952.

From inspection it is seen that these numbers, representing positions in the table, occur in pairs and (A_8+A_8') may be factored out of these pairs. This operation yields, as the final equations:

$$\begin{aligned}\Delta B_1 = {} & A_7'A_6'A_5A_4A_3'A_2'A_1 + A_7'A_6A_5'A_4A_3'A_2A_1 \\ & + A_7'A_6A_5A_4A_3'A_2'A_1' + A_7A_6A_5'A_4'A_3A_2'A_1 \\ & + A_7A_6'A_5A_4'A_3'A_2A_1 + A_7A_6'A_5'A_4'A_3A_2A_1', \quad (1)\end{aligned}$$

$$\Delta B_2 = A_7'A_6A_5'A_4A_3'A_2A_1 + A_7A_6'A_5A_4'A_3'A_2A_1, \quad (2)$$

$$\Delta C = A_7A_6'A_5'A_4'A_3A_2A_1'. \quad (3)$$

Variable Rate Counter

One way to design a counter which will count in steps of 0, 1, 2 or 3, is to use a 2-bit adder-subtractor with a gated counter which can count up or down.

Adder

The *addition* truth table is given in Table III. S_2 and S_1 are given before and after addition; *i.e.*, time $=t$ and time $=t+\tau$ where τ is the clock interval. Inspection of Table III shows that the following equations hold.

$$\Delta S_1(+) = B_1, \quad (4)$$

$$\begin{aligned}\Delta S_2(+) &= B_2'B_1S_1 + B_2B_1' + B_2B_1S_1' \\ &= B_2'B_1S_1 + B_2(B_1' + B_1S_1') \\ &= B_2'B_1S_1 + B_2B_1' + B_2S_1', \quad (5)\end{aligned}$$

$$\begin{aligned}k(+) &= B_2'B_1S_2S_1 + B_2S_2 + B_2B_1S_1 \\ &= B_1S_1(B_2 + B_2'S_2) + B_2S_2 \\ &= B_1B_2S_1 + B_1S_1S_2 + B_2S_2. \quad (6)\end{aligned}$$

TABLE I

A FUNCTION TABLE FOR THE FIRST QUADRANT

θ = ANGLE P = SIGN OF SINE θ C = SIGN OF SLOPE

A = CONTROL COUNTER S = SINE θ B = SLOPE

θ Degrees	θ in units of (360/256)°	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	P	S_7	S_6	S_5	S_4	S_3	S_2	S_1	C	B_2	B_1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1.4	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	1	1
2.8	2	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	1	1
4.2	3	0	0	0	0	0	0	1	1	0	0	0	0	1	0	0	1	0	1	1
5.6	4	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	1	1
7.0	5	0	0	0	0	0	1	0	1	0	0	0	0	1	1	1	1	0	1	1
8.4	6	0	0	0	0	0	1	1	0	0	0	0	1	0	0	1	0	0	1	1
9.8	7	0	0	0	0	0	1	1	1	0	0	0	1	0	1	0	1	0	1	1
11.3	8	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0	1	1
12.7	9	0	0	0	0	1	0	0	1	0	0	0	1	1	0	1	1	0	1	1
14.1	10	0	0	0	0	1	0	1	0	0	0	0	1	1	1	1	0	0	1	1
15.5	11	0	0	0	0	1	0	1	1	0	0	1	0	0	0	0	1	0	1	1
16.9	12	0	0	0	0	1	1	0	0	0	0	1	0	0	1	0	0	0	1	1
18.3	13	0	0	0	0	1	1	0	1	0	0	1	0	0	1	1	1	0	1	1
19.7	14	0	0	0	0	1	1	1	0	0	0	1	0	1	0	1	0	0	1	1
21.1	15	0	0	0	0	1	1	1	1	0	0	1	0	1	1	0	1	0	1	1
22.5	16	0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1
23.9	17	0	0	0	1	0	0	0	1	0	0	1	1	0	0	1	1	0	1	1
25.3	18	0	0	0	1	0	0	1	0	0	0	1	1	0	1	1	0	0	1	1
26.7	19	0	0	0	1	0	0	1	1	0	0	1	1	1	0	0	1	0	1	1
28.1	20	0	0	0	1	0	1	0	0	0	0	1	1	1	1	0	0	0	1	1
29.5	21	0	0	0	1	0	1	0	1	0	0	1	1	1	1	1	1	0	1	1
30.9	22	0	0	0	1	0	1	1	0	0	1	0	0	0	0	1	0	0	1	1
32.3	23	0	0	0	1	0	1	1	1	0	1	0	0	0	1	0	1	0	1	1
33.8	24	0	0	0	1	1	0	0	0	0	1	0	0	1	0	0	0	0	1	1
35.2	25	0	0	0	1	1	0	0	1	0	1	0	0	1	0	1	1	0	1	1
36.6	26*	0	0	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	1	0
38.0	27	0	0	0	1	1	0	1	1	0	1	0	1	0	0	0	0	0	1	0
39.4	28	0	0	0	1	1	1	0	0	0	1	0	1	0	0	1	0	0	1	0
40.8	29	0	0	0	1	1	1	0	1	0	1	0	1	0	1	0	0	0	1	0
42.2	30	0	0	0	1	1	1	1	0	0	1	0	1	0	1	1	0	0	1	0
43.6	31	0	0	0	1	1	1	1	1	0	1	0	1	1	0	0	0	0	1	0
45.0	32	0	0	1	0	0	0	0	0	0	1	0	1	1	0	1	0	0	1	0
46.4	33	0	0	1	0	0	0	0	1	0	1	0	1	1	1	0	0	0	1	0
47.8	34	0	0	1	0	0	0	1	0	0	1	0	1	1	1	1	0	0	1	0
49.2	35	0	0	1	0	0	0	1	1	0	1	1	0	0	0	0	0	0	1	0
50.6	36	0	0	1	0	0	1	0	0	0	1	1	0	0	0	1	0	0	1	0
52.0	37	0	0	1	0	0	1	0	1	0	1	1	0	0	1	0	0	0	1	0
53.4	38	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	0
54.8	39	0	0	1	0	0	1	1	1	0	1	1	0	1	0	0	0	0	1	0
56.2	40	0	0	1	0	1	0	0	0	0	1	1	0	1	0	1	0	0	1	0
57.7	41	0	0	1	0	1	0	0	1	0	1	1	0	1	1	0	0	0	1	0
59.1	42	0	0	1	0	1	0	1	0	0	1	1	0	1	1	1	0	0	1	0
60.5	43	0	0	1	0	1	0	1	1	0	1	1	1	0	0	0	0	0	1	0
61.9	44*	0	0	1	0	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1
63.3	45	0	0	1	0	1	1	0	1	0	1	1	1	0	0	1	1	0	0	1
64.7	46	0	0	1	0	1	1	1	0	0	1	1	1	0	1	0	0	0	0	1
66.1	47	0	0	1	0	1	1	1	1	0	1	1	1	0	1	0	1	0	0	1
67.5	48	0	0	1	1	0	0	0	0	0	1	1	1	0	1	1	0	0	0	1
68.9	49	0	0	1	1	0	0	0	1	0	1	1	1	0	1	1	1	0	0	1
70.3	50	0	0	1	1	0	0	1	0	0	1	1	1	1	0	0	0	0	0	1
71.7	51	0	0	1	1	0	0	1	1	0	1	1	1	1	0	0	1	0	0	1
73.1	52	0	0	1	1	0	1	0	0	0	1	1	1	1	0	1	0	0	0	1
74.5	53	0	0	1	1	0	1	0	1	0	1	1	1	1	0	1	1	0	0	1
75.9	54	0	0	1	1	0	1	1	0	0	1	1	1	1	1	0	0	0	0	1
77.3	55	0	0	1	1	0	1	1	1	0	1	1	1	1	1	0	1	0	0	1
78.8	56	0	0	1	1	1	0	0	0	0	1	1	1	1	1	1	0	0	0	1
80.2	57*	0	0	1	1	1	0	0	1	0	1	1	1	1	1	1	1	0	0	0
81.6	58	0	0	1	1	1	0	1	0	0	1	1	1	1	1	1	1	0	0	0
83.0	59	0	0	1	1	1	0	1	1	0	1	1	1	1	1	1	1	0	0	0
84.4	60	0	0	1	1	1	1	0	0	0	1	1	1	1	1	1	1	0	0	0
85.8	61	0	0	1	1	1	1	0	1	0	1	1	1	1	1	1	1	0	0	0
87.2	62	0	0	1	1	1	1	1	0	0	1	1	1	1	1	1	1	0	0	0
88.6	63	0	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	0	0
90.0	64	0	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0

* Indicates location of slope change.

TABLE II

A Table Showing the Values of the Angle and the Control Counter Where B_1, B_2, and C Change

θ in units $\left(\frac{360}{256}\right)^\circ$	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	
25	0	0	0	1	1	0	0	1	ΔB_1 (changes in B_1)
43	0	0	1	0	1	0	1	1	
56	0	0	1	1	1	0	0	0	
70	0	1	0	0	0	1	1	0	
83	0	1	0	1	0	0	1	1	
101	0	1	1	0	0	1	0	1	
153	1	0	0	1	1	0	0	1	
171	1	0	1	0	1	0	1	1	
184	1	0	1	1	1	0	0	0	
198	1	1	0	0	0	1	1	0	
211	1	1	0	1	0	0	1	1	
229	1	1	1	0	0	1	0	1	
43	0	0	1	0	1	0	1	1	ΔB_2 (changes in B_2)
83	0	1	0	1	0	0	1	1	
171	1	0	1	0	1	0	1	1	
211	1	1	0	1	0	0	1	1	
70	0	1	0	0	0	1	1	0	ΔC (changes in C)
198	1	1	0	0	0	1	1	0	

TABLE III

Addition Truth Table For B_1, B_2, and S_1, S_2

B_2	B_1	(at time t)		carry	(at time $t+\tau$)		ΔS_2	ΔS_1
		S_2	S_1	$k(+)$	S_2	S_1		
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0	0
0	0	1	0	0	1	0	0	0
0	0	1	1	0	1	1	0	0
0	1	0	0	0	0	1	0	1
0	1	0	1	0	1	0	1	1
0	1	1	0	0	1	1	0	1
0	1	1	1	1	0	0	1	1
1	0	0	0	0	1	0	1	0
1	0	0	1	0	1	1	1	0
1	0	1	0	1	0	0	1	0
1	0	1	1	1	0	1	1	0
1	1	0	0	0	1	1	1	1
1	1	0	1	1	0	0	0	1
1	1	1	0	1	0	1	1	1
1	1	1	1	1	1	0	0	1

Subtractor

The *subtraction* truth table is given in Table IV. From Table IV we derive the following equations.

$$\Delta S_1(-) = B_1, \tag{7}$$

$$\begin{aligned}\Delta S_2(-) &= B_2'B_1S_1' + B_2B_1' + B_2B_1S_1 \\ &= B_2'B_1S_1' + B_2B_1' + B_2S_1 \qquad (8)\\ &= B_2'B_1S_2'S_1' + B_2B_1'S_2' + B_2B_1S_2' + B_2B_1S_1' \\ &= B_1S_1'(B_2 + B_2'S_2') + B_2S_2'(B_1' + B_1) \\ &= B_1B_2S_1' + B_1S_1'S_2' + B_2S_2'. \qquad (9)\end{aligned}$$

Addition is indicated by $C=0$, subtraction by $C=1$. The complete change equations therefore are:

TABLE IV

Subtraction Truth Table For B_1, B_2 and S_1, S_2

B_2	B_1	(at time t)			(at time $t+\tau$)		ΔS_2	ΔS_1
		S_2	S_1	$k(-)$	S_2	S_1		
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0	0
0	0	1	0	0	1	0	0	0
0	0	1	1	0	1	1	0	0
0	1	0	0	1	1	1	1	1
0	1	0	1	0	0	0	0	1
0	1	1	0	0	0	1	1	1
0	1	1	1	0	1	0	0	1
1	0	0	0	1	1	0	1	0
1	0	0	1	1	1	1	1	0
1	0	1	0	0	0	0	1	0
1	0	1	1	0	0	1	1	0
1	1	0	0	1	0	1	0	1
1	1	0	1	1	1	0	1	1
1	1	1	0	1	1	1	0	1
1	1	1	1	0	0	0	1	1

$$\Delta S_1 = B_1, \tag{10}$$

$$\begin{aligned}\Delta S_2 &= C'\Delta S_2(+) + C\Delta S_2(-) \\ &= B_2'B_1(C'S_1 + CS_1') + B_2B_1' + B_2(C'S_1' + CS_1), \qquad (11)\\ k &= C'k(+) + Ck(-) \\ &= B_1B_2(C'S_1 + CS_1') + B_1(C'S_1S_2 + CS_1'S_2'). \qquad (12)\end{aligned}$$

Up-Down Counter

The remainder of the sine counter, $S_7 - S_3$, is simply a gated parallel counter. The count up equations are:

$$\Delta_U S_3 = C'k(+), \tag{13}$$

$$\Delta_U S_4 = S_3C'k(+), \tag{14}$$

$$\Delta_U S_5 = S_4S_3C'k(+), \tag{15}$$

$$\Delta_U S_6 = S_5S_4S_3C'k(+), \tag{16}$$

$$\Delta_U S_7 = S_6S_5S_4S_3C'k(+). \tag{17}$$

The count down equations are:

$$\Delta_D S_3 = Ck(-), \tag{18}$$

$$\Delta_D S_4 = S_3'Ck(-), \tag{19}$$

$$\Delta_D S_5 = S_4'S_3'Ck(-), \tag{20}$$

$$\Delta_D S_6 = S_5'S_4'S_3'Ck(-), \tag{21}$$

$$\Delta_D S_7 = S_6'S_5'S_4'S_3'Ck(-). \tag{22}$$

The complete counter equations are:

$$\Delta S_3 = C'k(+) + Ck(-) = k, \tag{23}$$

$$\Delta S_4 = S_3C'k(+) + S_3'Ck(-), \tag{24}$$

$$\Delta S_5 = S_4S_3C'k(+) + S_4'S_3'Ck(-), \tag{25}$$

$$\Delta S_6 = S_5S_4S_3C'k(+) + S_5'S_4'S_3'Ck(-), \tag{26}$$

$$\Delta S_7 = S_6S_5S_4S_3C'k(+) + S_6'S_5'S_4'S_3'Ck(-). \tag{27}$$

The only remaining task is to write the equation for ΔP. By considering where the sine changes sign one gets

$$\Delta P = x_8 x_7' x_6' x_5' x_4' x_3' x_2' x_1' + x_8' x_7 x_6 x_5 x_4 x_3 x_2 x_1. \quad (28)$$

Fig. 4 is a block diagram of information flow. The control counter is shown as a serial counter although it may be replaced by a parallel counter. Also, the diode nets are shown as clocked, although in practice it may be the flip-flops which are clocked. Similar results would have been obtained if set and reset equations had been used instead of change equations.

Applications

This same method may be extended to generate other variables by changing slope counter equations. Also, for situations where a closer approximation is necessary, slopes with multiples of (1/256) or (1/512) etc., could be used. But it would be necessary to use a 3- or 4-bit adder instead of the simple 2-bit adder shown.

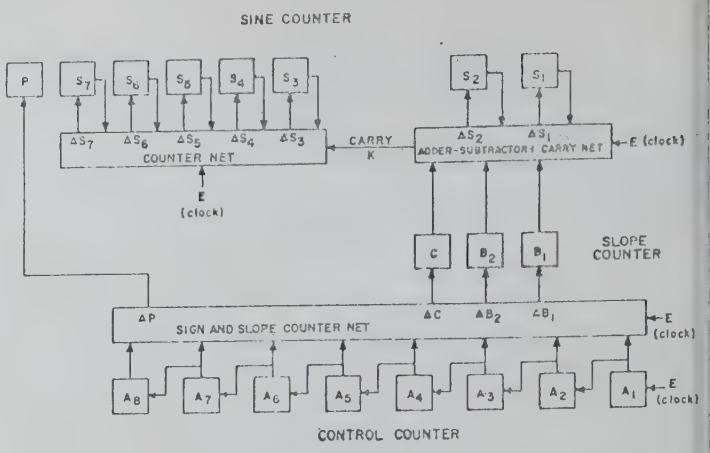

Fig. 4—Block diagram of information flow in the programmed counter for generating the sine function.

A Time-Division Multiplier*

M. LEJET LILAMAND†

Summary—A time-division multiplier for analog computers is described. Its features, for a switching pulse frequency of 2,000 cycles per second, are as follows: an accuracy of one part in a thousand, a pass band of 2 cycles per second, an input impedance of one megohm, and a very low output impedance (the output impedance of a feedback amplifier).

This multiplier has the following advantages when compared to two other types of analog multipliers: a) an accuracy limited solely by the stability of the components used and the fineness of the adjustments that can be made; b) a pass band greater than that of servomechanism multipliers; c) a much smaller amount of material than is necessary for diode multipliers with translators having parabolic characteristics and adjustments which can be made much more rapidly (although requiring a certain amount of practice); d) the possibility of changing the diodes without having to repeat all the adjustments.

These results have been obtained by the development of a precision electronic switch and by compensation of the stray capacities of the tubes.

Introduction

IN ANALOG computing machines, the primary form of nonlinear operation is multiplication. The Société d'Électronique d'Automatisme uses three types of multipliers: the servomechanism multiplier; the diode multiplier driving a translator having a parabolic characteristic; and finally, the modulation or time-division multiplier which is the subject of this article. This latter multiplier is of interest because it is more precise than the servomechanism multiplier. It is distributive and it requires much less material than the diode multiplier.

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The basic idea resides in the product of two modulations, one of the pulse-duration and the other of amplitude, of the form proposed in particular by Goldberg.

The multipliers based upon this principle[1] have, until the present time, been of insufficient accuracy or else they have been much too complex. At the Société d'Électronique d'Automatisme we have found a solution which is both economical and precise and which was made possible by the development of a precision electronic switch[2] and by the compensation of the stray capacities of the tubes.

We have also been able to obtain an accuracy of 0.1 per cent for an average switching pulse frequency of 1.5 kc.

Principle of Operation

The simplified schematic shown in Fig. 1 does not correspond exactly to the actual circuit, but it allows a clearer understanding of the principle of operation.

E_0 is a reference voltage ($E_0 = 100$ volts).

x and y are the two numbers, having values between -1 and $+1$, which are to be multiplied.

$E(x, y)$ and $E'(x, y)$ are the inputs (having values between 0 and E_0) to the switches W and W'.

Z and Z' are two other continuous inputs.

W and W' are two electronic switches controlled in synchronism by the flip-flop circuit B. (Actually, B

[1] See the bibliography.

[2] F. H. Raymond, "Improvements in electronic switching," Patent P.V. 658.091, November 13, 1953, and F. H. Raymond and M. B. Lejet, "Improvements applied to electronic switches," Patent P.V. 659.013, November 28, 1953.

consists of a sensing device—the flip-flop proper and a power stage.)

The operation is such that the output voltage U of the integrator A oscillates between two limits, U_1 and U_2, which are fixed in advance by the flip-flop and which are reached successively.

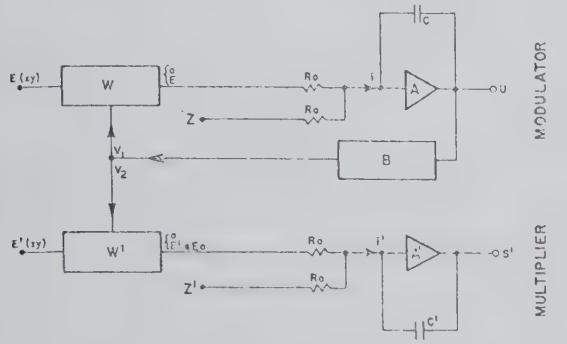

Fig. 1—Schematic diagram showing the operating principles of a time-division multiplier.

In order to clarify the operation, let us consider it as taking place in two phases:

Phase I: B delivers the control voltage $V_c = V_1$, W delivers voltage 0, W' delivers voltage 0.

Phase II: B delivers the control voltage $V_c = V_2$, W delivers voltage E, W' delivers voltage E'.

Let us consider the multiplier in operation. At the instant of time t_0+0, $U=U_2$ and B has just flipped. This is the beginning of the first phase (Fig. 2).

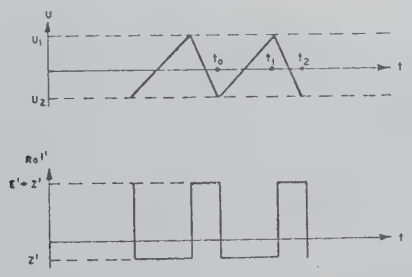

Fig. 2—Switching of the signal with time. U is the output voltage of the modulator, $R_0 i'$ is the input voltage to the multiplier.

Phase I:

$$U = U_2 - \frac{1}{R_0 C}\int_{t_0}^{t} Z\,dt \qquad t_0 \geqq t.$$

If we keep $Z<0$, U increases. Let t_1 be the instant at which $U=U_1$. We then have:

$$U_1 = U_2 - \frac{1}{R_0 C}\int_{t_0}^{t_1} Z\,dt.$$

Let us take the time $T_1 - t_0$ sufficiently small so that Z may be considered constant:

$$U_1 = U_2 - \frac{1}{R_0 C} Z T_1. \tag{1}$$

At time t_1, a new switching action takes place and the system enters its second phase.

Phase II:

$$U = U_1 - \frac{1}{R_0 C}\int_{t_0}^{t} (E+Z)\,dt.$$

If we keep $(E+Z)>0$, U decreases until time t_2 at which $U=U_2$. We have then:

$$U_2 = U_1 - \frac{1}{R_0 C}\int_{t_1}^{t_2} (E+Z)\,dt$$

$$= U_1 - \frac{1}{R_0 C}(E+Z)T_2. \tag{2}$$

B flips and the cycle starts over again.

Eqs. (1) and (2) may be written as follows:

$$\lambda = R_0 C(U_1 - U_2) = -ZT_1 = (E+Z)T_2,$$

from which:

$$-\frac{Z}{T_2} = \frac{E+Z}{T_1} = \frac{E}{T_1+T_2}$$

$$\frac{T_1}{T_1+T_2} = \frac{E+Z}{E} \tag{3}$$

$$\frac{T_2}{T_1+T_2} = -\frac{Z}{E}, \tag{4}$$

and the switching frequency is:

$$F = \frac{1}{T_1+T_2} = \frac{1}{\lambda\left(\frac{1}{-Z}+\frac{1}{E+Z}\right)} = \frac{-Z(E+Z)}{\lambda E}. \tag{5}$$

The average value, during one cycle, of the current i' which enters the integrator A' is:

$$i_m' = \frac{1}{R_0}\left(\frac{E'T_2}{T_1+T_2}+Z'\right) = \frac{1}{R_0}\left(-Z\frac{E'}{E}+Z'\right).$$

The input voltage to the multiplier, referred to a resistance R_0, is:

$$E_m' = R_0 i_m' = -Z\frac{E'}{E}+Z'.$$

It is desirable that this voltage be proportional to xy, in which case it is necessary that:

E be independent of x and of y, and of the form: $E=cE_0$;

Z be a linear function of x, of the form: $Z=(ax-b)E_0$;

E' be a linear function of y, of the form: $E'=(a'y+b')E_0$.

(The signs of a and a' are unimportant. We may, for example, assume them to be positive.)

$$E_m' = \frac{(b-ax)(a'y+b)}{c}E_0 + Z'$$

$$= -\frac{aa'}{c}xy - \frac{ab'x - ba'y - bb'}{c}E_0 + Z'.$$

It is further necessary that:

$$Z' = \frac{ab'x - ba'y - bb'}{c}.$$

Let us find the optimum values for a, a', b, b', and c. It would be desirable to have $a'a/c$ as large as possible (amplifier A' operated with small gain); in other words, the two quantities a/c and a' must both be large. In addition, the coefficients a, a', etc., must obey the conditions previously encountered, namely:

switch inputs:

$$0 < E < E_0 \text{ or } 0 < c < 1$$

$$0 < E' < E_0 \text{ or } 0 < (b' - a') < (b' + a') < 1.$$

This latter condition may be written:

$$\begin{cases} a' < b' \\ (b' + a') < 1 \end{cases}$$

where a' is as large as possible. Thus, it is necessary to take $a' = b' = \frac{1}{2}$. On the other hand we have:

$$0 < \frac{T_1}{T_1 < T_2} < 1,$$

but since it could be inconvenient to have $T_1 = 0$ or $T_2 = 0$, we restrict ourselves as follows:

$$0.1 < \frac{T_1}{T_1 + T_2} < 0.9$$

$$0.1 < \frac{-Z}{E} < 0.9$$

$$0.1 < \frac{b - ax}{c} < 0.9$$

$$0.1 < \frac{b - a}{c} < \frac{b + a}{c} < 0.9$$

$$\left.\begin{aligned} \frac{a}{c} + \frac{b}{c} &< 0.9 \\ \frac{a}{c} - \frac{b}{c} &< -0.1 \end{aligned}\right\} \quad (6)$$

which yields:

$$a/c < 0.4.$$

We may take, for example, $c = 1$ and $a = \frac{1}{2}$ in order to have simple numbers. The inequalities (6) become:

$$\begin{cases} b/c < 0.9 - 0.33 \\ b/c > 0.1 + 0.33 \end{cases}$$

$$\text{or } 0.43 < b/c < 0.57.$$

Thus we can take the value $b/c = \frac{1}{2}$.

Summarizing, if we start with the following values:

$$a = \tfrac{1}{3} \qquad b = \tfrac{1}{2}$$

$$a' = \tfrac{1}{2} \qquad b' = \tfrac{1}{2}$$

and if input voltages (referred to a resistance R_0) are:

$$E = E_0, \qquad Z = \left(\frac{x}{3} - \frac{1}{2}\right) E_0 \quad (7)$$

$$E' = \frac{1 + y}{2} E_0 \quad Z' = \left(\frac{x}{6} - \frac{y}{4} - \frac{1}{4}\right) E_0, \quad (8)$$

then the average value of the input to the multiplier will be:

$$E_m = -\frac{xy}{6} E_0.$$

and it will suffice to set the amplifier A' for a gain of 6 in order to have it deliver an output of:

$$xyE_0.$$

Equipment

The multiplier consists of two parts: the modulator (upper part of Fig. 1), where the pulse width or duration is modulated, and the multiplier proper (lower part of Fig. 1) where the amplitude modulation takes place. The heart of both the modulator and the multiplier is the electronic switch.

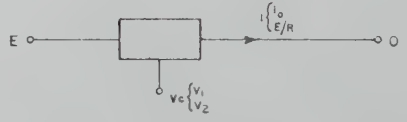

Fig. 3—Block diagram of a switch. E is the input, i is the output, V_c is the control voltage.

Electronic Switch Using Diodes

The operation of the electronic switch is shown in block form in Fig. 3.

At the input to the switch, we have a positive voltage E which varies from E_{min} to E_{max} (5 to 100 volts). At the output, we have zero voltage and a current i such that:

$i = i_0$ independent of E, when $V_c = V_1$;
$i = E/R$ proportional to E, when $V_c = V_2$.

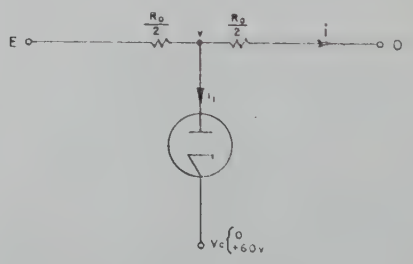

Fig. 4—Schematic diagram of a switch using a single diode.

The simplest system which comes to mind is that shown in Fig. 4.

Here $i = 0$ when $V_c = 0$ (diode is conducting) and $i = E/R_0$ when $V_c = +60v$ (diode is blocking).

In reality, when the diode conducts, the plate voltage of the diode is not actually zero. There is a residual voltage drop which is dependent upon E.

The current in the diode is:

$$i_1 = \frac{E - v}{\frac{R_0}{2}} - \frac{v}{\frac{R_0}{2}},$$

from which:

$$v = \frac{E}{2} - \frac{R_0}{4} i_1. \tag{9}$$

On the diode characteristic, shown in Fig. 5, we can see the variation Δv of v as E varies from E_{min} to E_{max}. If the characteristic were linear in this region, one could compensate for this variation, but it is not.

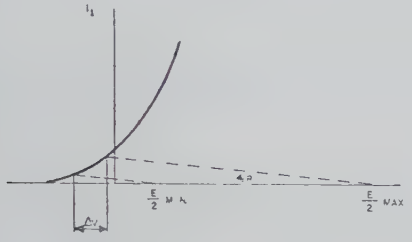

Fig. 5—Operating point of a switch using a single diode.

It can be shown that Δv reaches 250 mv under the following conditions:

Diode EB41: 6 volt filament,

$R_0 = 1$ megohm,

$5v < E < 100v$.

The switch which was finally decided upon, after what was believed to be a complete investigation of the subject, is shown in Fig. 6. It consists of two switches identical to the one just described. The second switch (consisting of R_2, R_3, and D_2 in Fig. 6) improves the characteristics of the first switch (consisting of R_1, R_2, and D_1 in Fig. 6) when both diodes are conducting.

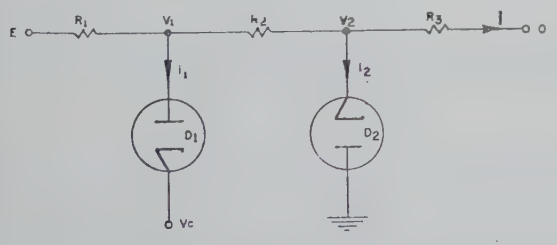

Fig. 6—Diagram of a switch using two diodes.

The first diode is biased negatively ($V_c = V_1 = -11v$) causing (when both diodes are conducting) a current i_2 to flow in the second diode which is independent of E. The operation may be seen on the graph of Fig. 7.

$$i_1 = \frac{E - v_1}{R_1} - \frac{v_1 - v_2}{R_2},$$

v_1 being the plate voltage of the first diode and

v_2 being the cathode voltage of the second diode.

One could begin by neglecting v_2 ($v_2 \approx 0.1$ volt) in order to compute v_1 ($v_1 \approx -11$ volts), from which we get:

$$v_1 = \frac{E}{1 + \frac{R_1}{R_2}} - i_1 \frac{1}{\frac{1}{R_1} + \frac{1}{R_2}} \tag{10}$$

which gives us the points A and B (Fig. 7). Moreover:

$$i_2 = \frac{v_1 - v_2}{R_2} - \frac{v_2}{R_3} \tag{11}$$

$$v_2 = \frac{v_1}{1 + \frac{R_2}{R_3}} - i_2 \frac{1}{\frac{1}{R_3} + \frac{1}{R_3}} \tag{12}$$

which gives us the points C and D (Fig. 7).

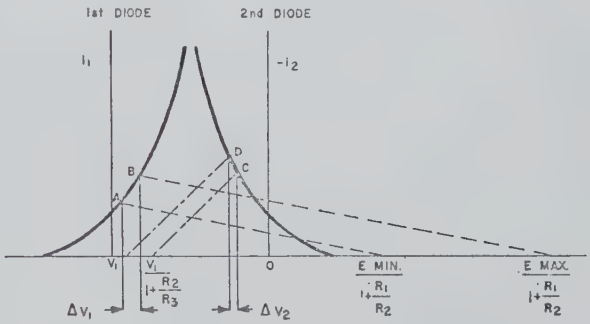

Fig. 7—Operating point of a switch using two diodes.

The variation Δv_2 of voltage v_2 will thus be less than 1 mv under the following conditions:

Diode EB41: 6 volt filament,

$5V < E < 100V$ $\quad v_1 = -11v$,

$R_1 = 0.5$ megohm, $\quad R_2 = 0.1$ megohm, $\quad R_3 = 0.4$ megohm.

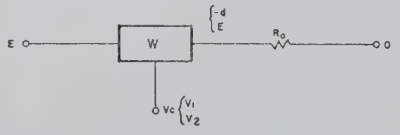

Fig. 8—Equivalent diagram of the switch.

Summarizing, the electronic switch (Fig. 8) will act as a resistance $R_0 = R_1 + R_2 + R_3$ to which a voltage is applied equal to:

$-d$ when $V_c = V_1$ (diodes conducting),

E when $V_c = V_2$ (diodes blocking),

where, by definition:

$$-d \times \frac{R_3}{R_1 + R_2 + R_3} = v_2. \tag{13}$$

The minus sign is chosen because in general v_2 is negative; in this case, since the current i_2 flowing through the

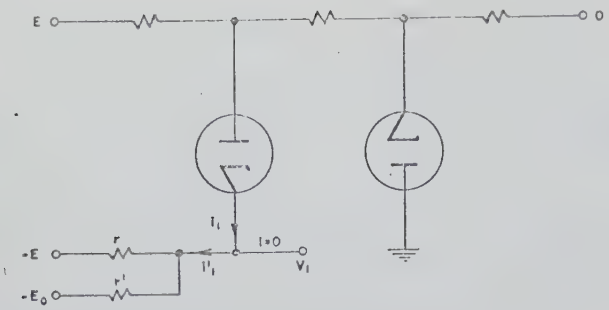

Fig. 9—Compensation of the current i_1 flowing through the diode, by a current i_1' having an opposite sense. V_1 is a source of voltage whose internal impedance is not zero.

second diode is independent of E, it is possible to cancel the residual voltage v_2 by connecting in series with the diode a variable resistance of the order of magnitude of the diode resistance without detracting from the qualities of the switch.

All this assumes that the voltage v_1 remains constant, whatever may be the value of the current i_1 flowing through the diode. In fact, the voltage source V_1 (cathodyne output of a power stage) has an internal resistance which is not negligible (5,000 ohms) and so, by using the arrangement shown in Fig. 9, a current i_1', equal to, and of opposite sign from, i_1, is caused to flow through the source simultaneously with current i_1, so that the total current will be approximately zero.

From (5):

$$i_1 \approx \frac{E}{R_1} - V_1\left(\frac{1}{R_1}+\frac{1}{R_2}\right), \tag{14}$$

$$i_1' = \frac{V_1+E}{r} + \frac{V_1+E_0}{r'}. \tag{15}$$

It is necessary that $i_1 \equiv i_1'$ for every value of E. In other words:

$$\begin{cases} R_1 = r & (16) \\ -V_1\left(\dfrac{1}{R_1}+\dfrac{1}{R_2}\right) = \dfrac{V_1}{r}+\dfrac{V_1+E_0}{r'} & (17) \end{cases}$$

$$r = R_1 \tag{18}$$

$$r' = \frac{E_0+V_1}{-V_1\left(\dfrac{2}{R_1}+\dfrac{1}{R_2}\right)} \quad (V_1 \text{ is negative}). \tag{19}$$

Modulator[3]

The modulator circuit is shown in Fig. 10.

During the period T_1, the diodes conduct and the input voltage, referred to a resistance R_0, is (Fig. 11):

$$\begin{array}{ll} \dfrac{xE_0}{3} & \text{for the first branch} \\ \dfrac{-(E_0-2d)}{2} & \text{for the second branch} \end{array}$$

[3] F. H. Raymond, "Driver for the electronic analogue computer, particularly for the multiplier," Patent P.V. 659.014, November 28, 1953.

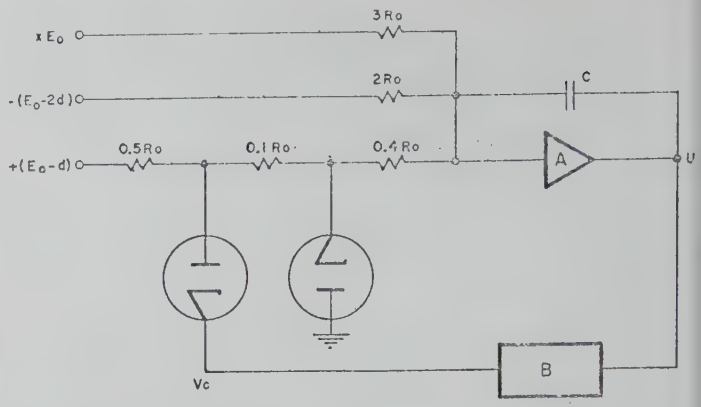

Fig. 10—Diagram of a modulator. A is an infinite gain amplifier shunted by C. B is a flip-flop with two stable stages.

$$\begin{array}{ll} -d & \text{for the third branch} \\ = \left(-\dfrac{1}{2}+\dfrac{x}{3}\right)E_0 & \text{for the total input.} \end{array} \tag{20}$$

During period T_2, the diodes are blocking and the input voltage, again referred to a resistance R_0, is (Fig. 11):

$$\begin{array}{ll} \dfrac{xE_0}{3} & \text{for the first branch} \\ \dfrac{-(E_0-2d)}{2} & \text{for the second branch} \\ +E_0-d & \text{for the third branch} \\ = \left(+\dfrac{1}{2}+\dfrac{x}{3}\right)E_0 & \text{for the total input.} \end{array} \tag{21}$$

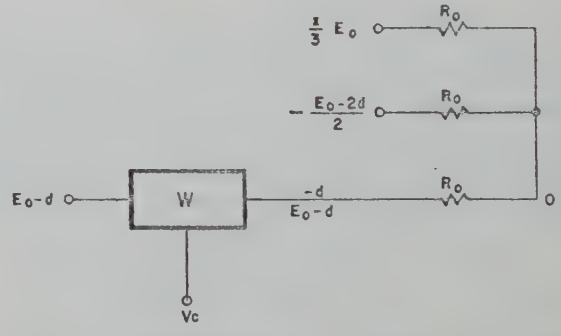

Fig. 11—Equivalent diagram of a modulator. The input resistances are taken as equal to R_0.

In practice, in order to obtain the voltages (E_0-d) and $-(E_0-2d)$, (where d is a positive voltage), the circuit shown in Fig. 12(a) is replaced by its equivalent circuit, Fig. 12(b), after properly adjusting the potentiometers $P+$ and $P-$ so as to produce the same current.

Referring now to the principle of operation mentioned earlier, while letting $E=E_0$ and $Z=(x/3)E_0-\frac{1}{2}(E_0-2d)-d=(x/3-\frac{1}{2})E_0$, (3) and (4) become:

$$\frac{T_1}{T_1+T_2} = \frac{1}{2}+\frac{x}{3} \tag{3'}$$

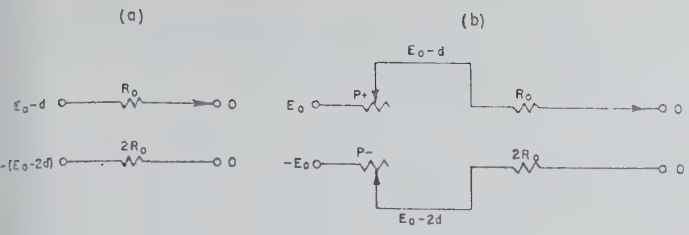

Fig. 12—Compensation of the voltage d

$$\frac{T_2}{T_1+T_2}=\frac{1}{2}-\frac{x}{3}. \qquad (4')$$

The pulse repetition frequency F can be calculated from (5). Thus, we find that:

$$F=\frac{1}{T_1+T_2}=\frac{E_0}{(U_1-U_2)R_0C}\left(\frac{1}{4}-\frac{x^2}{9}\right). \qquad (22)$$

This frequency may be varied by causing C to vary.

Multiplier

The multiplier circuit is shown in Fig. 13.

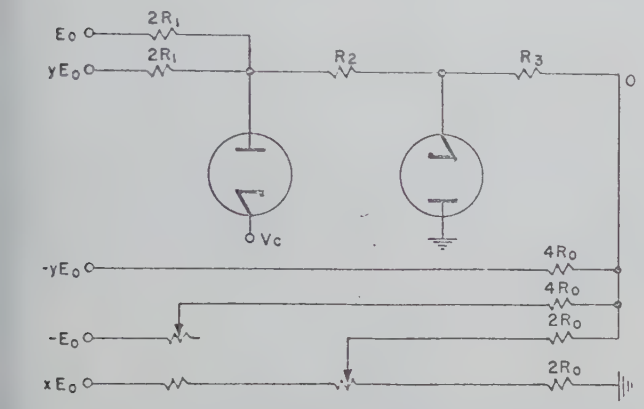

Fig. 13—Diagram of the multiplier. 0 is the grid (maintained at zero potential) of a negative feedback amplifier with an infinite gain.

Let us calculate the average input voltage E_m to the first branch, referred to a resistance R_0 (Fig. 14(a) and (b)):

Period T_1, diodes conducting, input $= -d'$

Period T_2, diodes blocking, input $=\frac{1}{2}(1+y)E_0$.

$$E_m=\frac{-d'T_1+\dfrac{1+y}{2}E_0T_2}{T_1+T_2}. \qquad (23)$$

By using (3') and (4'), it is found that

$$E_m=-\frac{xy}{6}E_0+\frac{y}{4}E_0-x\left(\frac{1}{6}+\frac{d'}{3E_0}\right)E_0+\left(\frac{1}{4}-\frac{d'}{E_0}\right)E_0. \qquad (24)$$

It will suffice to add three other unswitched inputs in order to compensate for all the terms which are different from $-(xy/6)E_0$ (as with the modulator, potentiometers are used to take the voltage containing d' into account). If the approximation $d'=0$ is made, the basic circuit of Fig. 1 is arrived at again. Note that the variation of y must be restricted within the following limits: $-0.9<y<+1.0$. In effect, the input to the switched branch, $E=\frac{1}{2}(1+y)E_0$, cancels for $y=-1$. The first diode is thus effectively blocked for $V_c=V_2(+70v)$ but the second diode loads up (zero potential difference between plate and cathode).

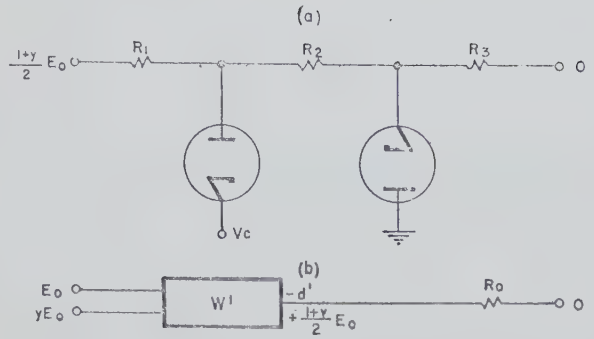

Fig. 14—(a) Switches branch of the multiplier; (b) Equivalent diagram of this branch, the input resistance taken as R_0.

With further reference to Fig. 1, according to whether the feedback circuit comprises a capacitor C' [Fig. 15(a)] or a resistor R [Fig. 15(b)] in parallel with a capacitor which is sufficiently large to act as a filter, voltages at the output S of the multiplier will be

$$S=\frac{1}{R_0C'}\int\frac{xy}{6}E_0dt \text{ or } S=\frac{R}{R_0}\frac{xy}{6}E_0, \text{ respectively.}$$

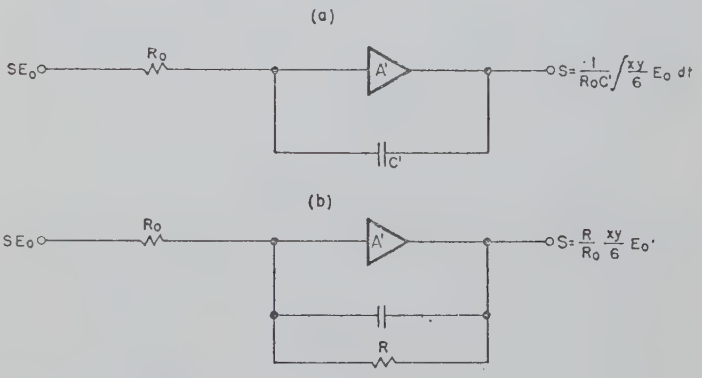

Fig. 15—Voltage at the output S of the multiplier. (a) Amplifier feedback via a capacitor; (b) amplifier feedback via a filter.

Compensation of Stray Capacities

The stray capacities are of the order of 5 pF. They produce important errors (several thousandths). They appear only because of the use of nonlinear elements. Fig. 16 shows the stray capacities C_1, C_2, C_3 of the modulator and C_1', C_2', C_3' of the multiplier.

Calculation of Time Constants: When the diodes are blocking, the capacities C_1, C_2, C_3 charge up and the current i does not reach its normal value instantaneously:

$$i=E/(R_1+R_2+R_3).$$

Thus the average value of i during the period T_2 is:

$$i = \frac{E}{R_1 + R_2 + R_3} - \frac{\Delta q}{T_2},$$

where Δq is the amount of electricity which serves to charge the stray capacities (to be calculated later).

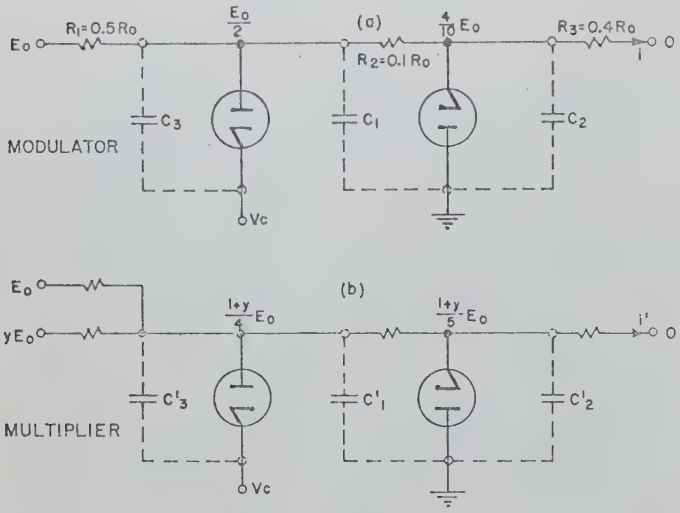

Fig. 16—Location of stray capacities (a) for the modulator and (b) for the multiplier.

When the diodes conduct, the capacities discharge across the diodes (low impedance) and the current i has for its normal value:

$$i = -d/(R_1 + R_2 + R_3).$$

We shall reexamine (1) and (2) which describe the operation of the modulator, but now we shall take Δq into account. For simplicity, we shall assume that the residual voltage d has been reduced to zero. We have:

$$\lambda = \left(\frac{1}{2} - \frac{x}{3}\right) T_1 = \left(\frac{1}{2} + \frac{x}{3}\right) T_2 - \Delta q \frac{R_0}{E_0},$$

from which:

$$\frac{\frac{1}{2} - \frac{x}{3}}{T_2} = \frac{\frac{1}{2} + \frac{x}{3} - \frac{\Delta q}{T_2}\frac{R_0}{E_0}}{T_1} = \frac{1 - \frac{\Delta q}{T_2}\frac{R_0}{E_0}}{T_1 + T_2}$$

$$\frac{T_2}{T_2 + T_1} = \frac{\frac{1}{2} - \frac{x}{3}}{1 - \frac{\Delta q}{T_2}\frac{R_0}{E_0}}$$

$$\approx \left(\frac{1}{2} - \frac{x}{3}\right)\left(1 + \Delta q \frac{R_0}{T_2 E_0}\right). \tag{25}$$

The term

$$\frac{\Delta q}{T_2}\frac{R_0}{E_0}$$

is a correction factor which is small compared to unity. In this factor, T_2 may be replaced by the value it has when there are no stray capacities:

$$\left(\frac{1}{2} - \frac{x}{3}\right)(T_1 + T_2) \quad \text{(refer to Fig 4)}.$$

Whence:

$$\frac{T_2}{T_1 + T_2} = \left(\frac{1}{2} - \frac{x}{3}\right)\left[1 + \frac{\Delta q R_0}{E_0\left(\frac{1}{2} - \frac{x}{3}\right)(T_1 + T_2)}\right]$$

$$= \left(\frac{1}{2} - \frac{x}{3}\right) + \Delta q \frac{R_0}{E_0} F,$$

where $F = \dfrac{1}{T_1 + T_2}$. (26)

Similarly, for (23) which describes the operation of the multiplier, we find (keeping $d' = 0$):

$$E_m = \frac{E_0\left(\frac{1+y}{2}\right) T_2 - \Delta g' R_0}{T_1 + T_2}$$

$$= E_0\left(\frac{1+y}{2}\right)\left(\frac{1}{2} - \frac{x}{3}\right) + \left(\frac{1+y}{2}\right)\Delta q R_0 F - \Delta q' R_0 F. \tag{27}$$

The error introduced by the capacities is thus:

$$\Delta E_m = R_0 F\left[\frac{1+y}{2}\Delta q - \Delta q'\right]. \tag{28}$$

Now we shall calculate Δq and $\Delta q'$, calling E the input to the switch ($E = E_0$ for the modulator and $E = \frac{1}{2}(1+y) \cdot E_0$ for the multiplier). The variation of charge for the capacity C_1 is:

$$\Delta Q_1 = C_1\left[E\frac{R_2 + R_3}{R_1 + R_2 + R_3} - V_1\right].$$

The quantity of electricity Δq_1, which will not pass through resistor R_3 because of the charge on C_1 is:

$$\Delta q_1 = \Delta Q_1 \frac{R_2}{R_2 + R_3} = C_1\left[E\frac{R_1}{R_0} - V_1\frac{R_1}{R_2 + R_3}\right]$$

where $R_0 = R_1 + R_2 + R_3$.

Similarly for capacities C_2 and C_3:

$$\begin{cases} \Delta Q_2 = C_2 E \dfrac{R_3}{R_0} \\ \Delta q_2 = \Delta Q_2 \dfrac{R_1 + R_2}{R_3} = C_2 E \dfrac{R_1 + R_2}{R_0} \end{cases}$$

$$\Delta Q_3 = C_3\left[E\frac{R_2 + R_3}{R_0} - V_2\right]$$

$$\Delta q_3 = \Delta Q_3 \frac{R_1}{R_2 + R_3} = C_3\left[E\frac{R_1}{R_0} - V_2\frac{R_1}{R_2 + R_3}\right].$$

Whence:

$$R_0 \Delta q = R_0(\Delta q_1 + \Delta q_2 + \Delta q_3)$$

$$= E[R_1 C_1 + (R_1 + R_2)C_2 + R_1 C_3]$$

$$- \frac{R_1 R_0}{R_2 + R_3}(V_1 C_1 + V_2 C_3). \tag{29}$$

This is of the general form:

$$R_0\Delta q = aE - bE_0$$

where

$$a = R_1C_1 + (R_1 + R_2)C_2 + R_1C_3, \tag{30}$$

$$b = \frac{R_1R_0}{R_2 + R_3}\left[\frac{V_1}{E_0}C_1 + \frac{V_2}{E_0}C_3\right]. \tag{31}$$

a and b are homogeneous with the time constants.

In the case of the modulator $E = E_0$, so that

$$q = (a - b)E_0.$$

In the case of the multiplier: $E = \frac{1}{2}(1+y)E_0$

$$q' = (\tfrac{1}{2}a'(1 + y) - b')E_0.$$

The error for the multiplier is:

$$\Delta E_m = F\left[\frac{1+y}{2}(a-b)E_0 - \left(a'\frac{1+y}{2} - b'\right)E_0\right]$$

$$= E_0F\left[\frac{1+y}{2}(a - a' - b) + b'\right]. \tag{32}$$

The frequency F being proportional to $(\frac{1}{4} - x^2/9)$ from (22), the capacities introduce errors in the terms containing $1, x^2, y, x^2y$.

Order of Magnitude of ΔE_m: Let us assume that the switch for the modulator is identical with the switch for the multiplier ($a = a'$, $b = b'$). An error exists of the order of magnitude of bE_0F.

Thus, if $F = 2{,}000$ cps (a large value of F is taken in order to increase the pass band of the multiplier):

$$R_1 = 0.5 \text{ meg } \Omega$$

$$R_2 = 0.1 \text{ megohm}$$

$$R_3 = 0.4 \text{ megohm}$$

$$C_1 = C_2 = C_3 = 5pF$$

$$V_1 = -11V$$

$$V_2 = +70V$$

and we have

$$\frac{\Delta E_m}{E_0} = bF = 6 \times 10^{-3}.$$

Let us examine the expression for the error ΔE_m, (32). In order to cancel ΔE_m, it is necessary, in the first place, to increase the modulator time constant by Δa so that:

$$a + \Delta a - a' - b = 0.$$

This is accomplished by inserting a variable capacitor C_0 in parallel with C_2. Thus we have:

$$\Delta a = (R_1 + R_2)C_0.$$

In the second place, it is necessary to compensate for the term E_0Fb'. This is simple because the signal fed into the cathode of the diode consists of rectangular pulses having a constant amplitude of $(V_2 - V_1)$ and a frequency F. It is sufficient to connect into the multiplier circuit (Fig. 17) a variable capacitor C_4' and a rectifier in order to obtain the proper sign.

The charge variation of the capacitor C_4' is:

$$\Delta Q_4 = C_4'(V_2 - V_1).$$

The charging current of the capacitor flows through the rectifier (which we will assume to be perfect) while the discharge current flows through resistor r. The average current $\Delta i_{4m}'$ which flows through r will be:

$$\Delta i_{4m}' = -FC_4'(V_2 - V_1). \tag{35}$$

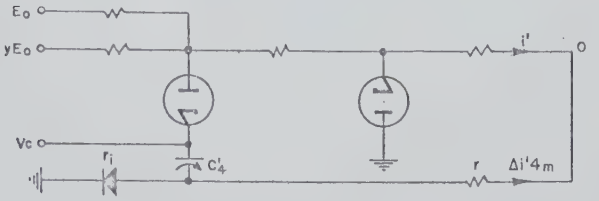

Fig. 17—Corrective capacitor C_4' connected in the multiplier.

This current adds to the multiplier current i'. It is equivalent to an input voltage of $\Delta i_{4m}'R_0$.

Thus it is necessary that:

$$b'E_0F - FC_4'(V_2 - V_1)R_0 = 0 \text{ and}$$

$$C_4' = \frac{b'E_0}{R_0(V_2 - V_1)}.$$

Method of Adjustment. It should be noted that the above mentioned capacities introduce errors which are proportional to the switching frequency F. In order to reduce the errors, it would be sufficient *a priori* to reduce the frequency, but in doing so, the pass band is simultaneously reduced since it is the average values of x and y during the periods T_1 and T_2 which are important.

For a frequency of 2,000 cps, the pass band is about 2 cps. In order to increase it, it is sufficient to decrease the value of the modulator feedback capacitor C.

Since a modulator must be capable of controlling several multipliers, the capacitor C_0 is given *a priori* a larger value, so that, whatever may be the multiplier:

$$a + \Delta a - a' - b > 0, \quad \text{where} \quad a = (R_1 + R_2)C_0.$$

If we replace F by its value in (32), then the input error is given by the following:

$$\Delta E_m = E_0\left(\frac{1}{4} - \frac{x^2}{9}\right)\frac{E_0}{(U_1 - U_2)R_0C}$$

$$\cdot\left[\frac{1+y}{2}(a + \Delta a - a' - b) + b'\right].$$

If the amplifier is adjusted for a gain of -6 in order to have $1 \times 1 = 1$, S may be written as follows:

$$S = xyE_0 - \frac{6E_0^2}{(U_1 + U_2)R_0C}\left(\frac{1}{4} - \frac{x^2}{9}\right)$$

$$\cdot\left[\left(\frac{a + \Delta a - a' - b}{2} + b'\right) + \frac{a + \Delta a - a' - b}{2}y\right]$$

$$S = xyE_0 + A\left(\frac{1}{4} - \frac{x^2}{9}\right) + B\left(\frac{1}{4} - \frac{x^2}{9}\right)y$$

where A and B are functions of time constants a, a', etc.

If we make the following products:

$$x = 0 \qquad y = +1$$
$$x = 0 \qquad y = -1$$

we shall find:

$$S_1 = \frac{A}{4} + \frac{B}{4}$$

$$S_2 = \frac{A}{4} - \frac{B}{4}.$$

Therefore: $B = 2(S_1 - S_2)$.

The term B can be compensated by adjusting the variable capacity C_0' which is connected in parallel with C_2' in the multiplier. In other words, the time constant a' is modified in such a way as to have:

$$S_1 - \frac{B}{4} = S_1 - \frac{S_1 - S_2}{2} = \frac{S_1 - S_2}{2}.$$

When B is compensated, we have:

$$S = xyE_0 + A\left(\frac{1}{4} - \frac{x^2}{g}\right);$$

for $x = 0$, $y = 0$ we shall find: $S_3 = A/4$.

This term can be cancelled by adjusting C_4'; in other words b', which does not change B.

It should be noted that it is necessary to make these adjustments only once, at the time when these equipments are placed in operation. All further drifting of the multiplier (caused by variations of resistance with temperature or aging of the diodes) does not involve any readjustment of the capacitors.

Example of the Use of a Modulation Multiplier

An essential property of the multiplier is its *distributivity*. This property is particularly useful when vector products are to be computed. In aerodynamics, for example, it is desired to obtain the integral of the components of vector products of the form:

$\overline{W} \times \overline{V}$ (in the equation for the magnitude of motion)
$\overline{W} \times \overline{H}$ (in the equation for kinetic moment).

If the components p, q, r of the vector $\overline{W}$ feed three modulators, the control voltage coming out of each modulator can control as many multipliers as may be necessary.

We see in Fig. 18 how to perform the multiplication $\overline{W} \times \overline{V}$, that is, how to find the components:

$$\begin{cases} qw - rv, \\ ru - pw, \\ pv - qu. \end{cases}$$

With the same modulators, but with three other multipliers, we can similarly find $\overline{W} \times \overline{H}$. To obtain the 12 products, we need the following equipment:

3 amplifiers and 3 modulators,
3 amplifiers and 6 multipliers (for $\overline{W} \times \overline{H}$),
3 amplifiers and 6 multipliers (for $\overline{W} \times \overline{V}$),

or a total of 9 amplifiers, 3 modulators, and 12 multipliers—whence the great economy in the number of necessary amplifiers and modulators.

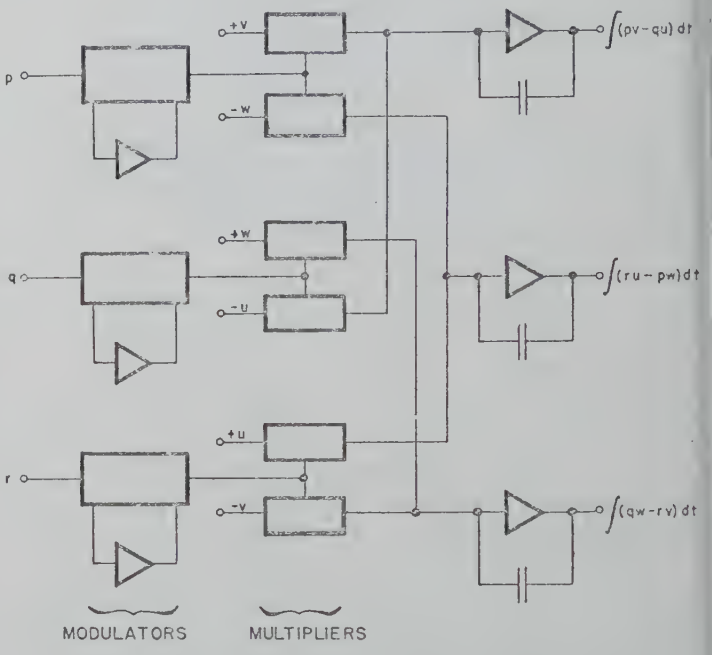

Fig. 18—Diagram illustrating the calculation of vector products.

Results and Conclusion

If the amplifier A' [Fig. 15(b)] is adjusted for a gain of 6 in order to have the following relation: $S = xyE_0$, the accuracy is $\Delta S/E_0 = 1/1{,}000 = 0.1$ per cent.

This accuracy is limited by the precision of the resistors and by the stability of the tubes (the variation of the diode characteristics because of aging or mechanical shock). The multiplier developed by Goldberg in the United States achieves independence of the tube characteristics by using current control rather than voltage control, but it has the disadvantage of requiring 6 amplifiers.

That is why, except for a slight decrease in accuracy, we undertook at Société d'Électronique d'Automatisme to find a simpler solution requiring only two amplifiers.

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As a member of the Theory Group of the Accelerator Project at the Brookhaven National Laboratory from 1947 to 1951, he was concerned with the theory and design of the Cosmotron, Brookhaven's three-billion-volt proton synchrotron. From 1951 to 1954, he was a member of the staff of the Mathematical Sciences Division of the Office of Naval Research, Washington, D. C., administering ONR's program of supported research in the fields of computers and mathematics. In this position, he compiled a number of surveys of various aspects of the digital-computer field, including the 1953 *ONR Survey of Automatic Digital Computers*, which covers the details of about a hundred machines.

In 1954, he joined the Systems Branch of Sylvania's Electronic Defense Laboratory, Mountain View, Calif., where he has been concerned mainly with communication theory and the design of electronic countermeasure systems.

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A Report on the International Analogy Computation Meeting*

N. M. BLACHMAN†

THE International Analogy Computation Meeting, held in Brussels, Belgium, September 27 to October 1, 1955, was organized by the Société Belge des Ingenieurs des Telecommunications et d'Électronique (SITEL) with the collaboration of the Société Belge des Electriciens (SBE) and Société Belge des Mecaniciens (SBM), under the patronage of the Belgian Ministries of Public Education, Economic Affairs, and Communication and the city of Brussels. With such auspicious sponsorship, the meeting would have been a success even without the presentation of any papers.

Everything was organized for the pleasure and convenience of the participants. There was a reception held by the Mayor at the City Hall on the first night of the meeting and another held by the engineering societies at the Hôtel Ravenstein on the third night of the meeting. There was to have been a concert at the National Broadcasting Institution on the second night, but it was unfortunately canceled. The closing banquet, held on the fourth and last night of the meeting at the Hôtel Métropole, will not soon be forgotten. Four wines were served, each with the appropriate courses, and the price of the banquet was only 200 Belgian francs ($4.00). The ladies who arranged the seating at the banquet were careful to make sure that those who sat next to each other knew some language in common. They assumed, quite successfully, that the Dutch and Americans know English.

Other noteworthy arrangements were the special post office, bank, and travel bureau set up in the building where the meeting was held, the premises of Fabrimétal, at 21, rue des Drapiers; the daily tea provided by the management of Fabrimétal; and the program for ladies, which each day offered trips to various sights and museums. Well-appointed discussion rooms, with stenographers available, were provided for the extension of the discussion of papers, and bilingual stenotypists were present at all sessions of the meeting to record the proceedings. The two official languages of the meeting were French and English; of the nearly one hundred papers, about half were presented in each language.

Speakers came from 13 different countries; participants, of whom there were 400, came from 18. In order of numbers of participants, these included: Belgium, France, the United Kingdom, Switzerland, the Netherlands, Sweden, Germany, the U. S., Italy, Spain, Yugoslavia, the U.S.S.R., Poland, Denmark, Norway, Canada, Australia, and Czechoslovakia. In numbers of speakers, Belgium ranked third and the U. S. fourth, the top four countries accounting for three fourths of the papers presented. Only one speaker, a Pole, came from east of the Curtain.

For most of the papers, 15 minutes were allotted for the presentation and five minutes for discussion. There were generally two simultaneous sessions for such short papers, divided roughly on the basis of subject matter, following each of the seven longer talks, for which one hour was allowed in a single session.

One-Hour Talks

Following the opening ceremonies at the Palais des Academies on Tuesday, September 27, F. H. Raymond, director of the Société d'Électronique et d'Automatisme, Paris, talked (in French) on "Electronic Differential Analyzers," tracing the history of these machines, and prognosticating their future development. He also considered the influence of digital computers and numerical analysis upon analog computing.

On Wednesday morning, E. L. Harder, Director of the Analytical Section of the Westinghouse Electric Corporation, Pittsburgh, under the title "Electrical Network Analyzers," described the six computing facilities currently in use by his organization: 1) a passive ac network calculator, capable of representing 36 generating stations; 2) a passive dc calculating board, used for the study of small power systems and for the solution of Laplace's and Poisson's equations; 3) the Anacom, a large-scale electric analog computer, consisting mostly of passive elements, used for the study of vibrations and transients in electrical circuits, mechanical systems, and fluid flow; 4) an electronic differential analyzer containing feedback amplifiers, arranged for handling up to three problems simultaneously; 5) an IBM Card-Programmed Calculator; and 6) an IBM Type 650 magnetic-drum computer. The latter two machines are to be replaced in January, 1956, by an IBM 704 Electronic Data-Processing Machine. Harder discussed types of problems assigned to each of these computers, including problems requiring use of more than one of them.

On Wednesday afternoon, Professor L. Malavard of Paris talked on "The Rheoelectric-Analogy Method, its Possibilities and Trends" (in French). He discussed various tanks that are used and automatic equipment for the tracing of equipotentials, gradients, etc., as well as the types of problems which are amenable to rheoelectric modeling. He suggested extension of the method by connecting external electrical set-ups to tanks.

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On Thursday morning, J. G. L. Michel of the National Physical Laboratory, Teddington, England, talked on "The Mechanical Differential Analyser: Recent Developments and Applications." He reviewed the history of these machines, leading up to the large servo-connected differential analyzer recently brought into use at NPL. It contains 20 integrators and is capable of solving three problems simultaneously. Michel discussed the types of problems for which such machines are suitable and suggested that two-boundary ordinary differential equations, eigenvalue problems, partial differential equations, integral equations, and algebraic and descriptive-geometric problems may also be solved by means of a differential analyzer.

Thursday afternoon, G. Liebmann of the Associated Electrical Industries' Research Laboratory, England, gave a very well received talk on "Resistance-Network Analogs" for the solution of partial differential equations, such as Poisson's equation in two dimensions. The truncation error of the finite-difference-equation approximation which is represented by the resistance network can be reduced by feeding auxiliary currents into the network nodes. In this way, an analog accurate to 0.01 per cent can be obtained. Liebmann discussed various applications of (x, y) and (r, z) resistance-network analogs and described recent extensions of the method to the biharmonic equation and the diffusion equation. For the solution of the equation $\nabla^2\mu=\mu$ in two dimensions, Liebmann suggested the use of two similar plane rectangular networks of resistances with corresponding points connected by additional resistances. The latter resistances must be chosen so as to yield a maximum accuracy of solution.

On Friday morning, Professor J. Brodin of the Laboratoire de Recherches Ballistiques et Aérodynamiques, Vernon, France, presented "A Concrete Way of Teaching Linear Operator Calculus" (in French), namely, the representation of linear operators by linear networks, in particular, representing the integrator by an amplifier with capacitive feedback. He also discussed the representation of operations upon operators, such as addition, multiplication, and inversion, and the convergence of a sequence of operators.

The last one-hour talk was given on Friday afternoon by Professor H. Wallman of the Chalmers Institute of Technology, Gothenburg, Sweden, on the topic "Special Computers." He described the Chalmers Institute's "electronic integral analyzer," which consists of an electronic differential analyzer plus a generator for functions (kernels) of two variables. (For details, see the remarks of V. Wentzel below.) This device is thus able to compute integral transforms, and the Hilbert transform, for example, has already been computed in this manner. Wallman also mentioned the passive network analyzer at the High-Voltage Laboratory of the Chalmers Institute, which is used in the study of power-distribution systems. The most noteworthy feature of this analyzer is the rotation by 90° of the angles of the impedances, so that inductances, of which there are many, become resistances in the analyzer, resistances are represented by capacitances, and capacitances become negative resistances, of which only a few are required. Inductances are not required in the analyzer. Wallman also mentioned the "Complex-Plane Analyzer," which permits the multiplication and division of complex numbers, and, therefore, the exploration of the behavior of polynomials in the complex plane, by using the polar representation for complex numbers, and applying the angle to a linear potentiometer and the radius vector to a logarithmic potentiometer, whose outputs are stored on capacitors.

Short Papers

The ninety short papers dealt with a wide variety of topics, including: various electronic differential analyzers, rheoelectric analogs, resistive networks for the solution of both ordinary and partial differential equations, techniques for constructing multipliers and function generators, methods for the solution of algebraic equations and for finding the eigenvalues of matrices, studies of the mathematical foundations of analog computation and the accuracy of its results, components for mechanical as well as for electronic analog computers, miniature power networks which include miniature turbines, three-phase rotating machines, transformers, power lines, etc.; and the application of analog computers to investigations relating to aerodynamics, fluid flow, structures, nuclear reactors, transistors, and the paths of particles in electromagnetic fields. It would not be feasible to discuss all of these short papers, but the following are among the more interesting.

J. F. Coales of the Cambridge University Engineering Department talked on "The Use of Computing Elements in Control Systems," whereby a control system optimizes its own performance by accommodating to the autocorrelation function of its input. He stressed the case of on-off control systems, in which a settling time comparable with that of a linear system can be obtained with half the maximum torque of the latter. The resulting saving might far outweigh the cost of the necessary computing circuits.

M. E. Fisher of the Department of Physics, King's College, London, discussed "Higher-Order Differences in the Analog Solution of Partial Differential Equations," showing that in this way the number of interpolation stations required for a given accuracy in a typical problem may readily be reduced to one third of the total normally needed.

Function Generators

W. W. Seifert of the M.I.T. Dynamic Analysis and Control Laboratory spoke on "The Generation of Functions of Two Independent Variables," mentioning 1) the use of a photoformer with a mask whose density is $f(x, y)$, 2) the diode-network technique developed by the Reeves Instrument Co., and 3) the technique, de-

veloped at the D.A.C.L., of using a low-shrinkage plaster to model a surface $z=f(x, y)$, on which a stylus having a 1/16-inch tip and operating a rectilinear potentiometer is positioned at (x, y). A 0.1 per cent accuracy is obtainable where the inclination of the surface is 30°, 1.5 per cent where it is 70°. It was claimed that the plaster can be molded to an accuracy of 1 per cent without undue difficulty. The cut-off frequency of this function generator exceeds 20 cps. Four such generators have been built at a cost of $150,000. During the discussion which followed the paper, the suggestion was made that a function of two variables may alternatively be generated digitally, with analog-digital conversion at the input and output.

G. D. Bergman of Fairey Aviation, England, reported on "A New Electronic Analog Storage Device" which uses the physical principles of Williams cathode-ray-tube storage. The device records a voltage waveform of about a millisecond's duration and can reproduce it after a time lapse of the order of milliseconds. It is particularly useful in the solution of difference-differential equations, where the solution obtained in one cycle of operation is required during the next cycle.

V. Wentzel of the Chalmers Institute of Technology, Gothenburg, Sweden, described two "Electronic Function Generators." The first generates $f(x, y)$ by means of a photographic plate, effectively 6×4 cm, divided into thirty 2-mm columns, each for a different x value. The function is given by the width (at most 1 mm) of the transparent area in the column at the height y. The columns are saw-tooth scanned by a flying-spot scanner and photocell, to yield width-modulated pulses, which are easily used in multiplication. The device has a brightness stabilizing loop; its error, due to the nonlinearity of the scan, is about 1 per cent. The vertical resolution is about 1 mm, and the scanning time for the whole plate is 3.5 seconds. The second function generator, yielding a function of time $f(t)$, switches an integrator input by means of dekatrons to successive values of df/dt which are set on thirty potentiometers. An accuracy of 0.2 per cent is claimed for this device.

E. Elgeskog of the same laboratory presented an analysis of the photoformer as a curve follower, in which he emphasized the desirability of inserting a low-pass filter in its output in order to attenuate the noise due to the photocell. He has succeeded in building a photoformer with an accuracy of 1 per cent, a bandwidth of 10 kc, and a noise level of 10 mv, to be compared with a maximum output-signal level of ±30 v.

Multipliers

G. Piel of the Société d'Électronique et d'Automatisme, near Paris, presented a paper on "Digital-Analog Conversion by Means of a Relay Decoder," which involves the use of the "cyclic" or "Gray" code, so that only one relay switches at a time, and there is never a large jump in the output voltage due to nonsimultaneous switching as the input changes continuously. The converter can also serve as a multiplier if the multiplicand is fed to the decoding circuit as the reference voltage. Such a device has been built with a precision of 11 binary digits and is capable of switching 200 times per second. A single cyclic code is used to control and serve as multiplier for many such multiplying circuits.

F. W. Gundlach of the Technische Universitaet in Berlin described "A New Electron-Beam Multiplier with an Electrostatic Hyperbolic Field," which subjects the beam first to a uniform deflecting field (multiplier), then to a hyperbolic field (multiplicand), then to another uniform field (the product), which, through a feedback loop, counteracts the horizontal deflection due to the hyperbolic field, which is proportional to both the vertical deflection the beam had on entering the hyperbolic field and the strength of the latter field itself. This multiplier is capable of four-quadrant operation without additional complications, and it is easily converted to a divider. The axes of the electrodes must be accurately aligned, though by the application of dc potentials it is possible to correct to a certain extent for errors. With these corrections applied, the device has an accuracy of 0.5 per cent. A 700-volt accelerating potential is used. The beam current is 15 microamperes: a larger current would be detrimental because of the resulting space-charge defocusing of the beam, which is very undesirable in the inhomogeneous field of the hyperbolic plates.

J. Isbeau of the Université Libre de Bruxelles described "An Analog Multiplier-Divider" which computes AB/C by shocking two identical oscillatory networks with pulses of sizes B and C, respectively, and measuring the amplitude of the voltage on the first when the voltage on the second equals A. A prototype has been built which operates 15,000 times per second with an accuracy of 2 per cent at dc and a 95 per cent response at 1 kc.

L. E. Lofgren of the Research Institute of National Defense, Stockholm, presented a paper on an "Analog Multiplier Based on the Hall Effect." Using an n-type germanium crystal, he has obtained an accuracy of 0.2 per cent for frequencies up to 10 kc with an input-voltage-frequency product no greater than 10 volt-kc on one input. The ranges of the input and output voltages are all ±40 volts.

Large Analog Computers

Of the considerable number of computers described at the meeting, one of the two largest was "The Wright Air Development Center's New Large Analog Computer," described by L. M. Warshawsky, Chief of the Analog Section of the WADC Aeronautical Research Laboratory, Dayton. This machine is being procured by the U. S. Air Force for WADC for use in the solution of problems associated with air-weapon systems. Besides being large (400 amplifiers) and accurate, this computer incorporates several novel features aimed at minimizing human-operator errors, checking the valid-

ity of the set-up, and operating the equipment in an optimum voltage range.

Special features of the machine include: 1) the problem-check mode, in which prescribed values are substituted for all variables and all outputs are printed out automatically; 2) plug-board verification; 3) automatic time-base change by a factor of two, effected by the throwing of a switch that doubles all capacitances; 4) minimum-excusion indication at the end of a run to show where the scale needs compression; 5) digital potentiometer-setting equipment, and print out of patched connections, including diode networks, at the rate of two or three minutes per patch board, there being eight boards altogether, each having 2,500 holes; 6) an "automatic programmer," which varies parameters systematically from run to run for 8,000 runs, each run taking 30 to 40 seconds; and 7) a digital voltmeter which has a static accuracy of 0.01 per cent.

This computer is under construction by the Reeves Instrument Company and is scheduled for delivery in June, 1956, at a price "slightly under $1 million." It will be set up in a 40×60-foot rectangle, lined by the four identical sections consisting of 14 relay racks each, into which the computer can be split for the solution of smaller problems. There is a fifth section which interconnects the other four and also contains additional equipment, such as a noise generator. The computer incorporates both electromechanical and quarter-square multipliers. Its amplifiers have a total gain of 6×10^7, 2×10^4 being in the operational amplifier and 3,000 in the chopper amplifier. The open-loop amplifier bandwidth is 20 kc 1 db down.

The computer is a little larger than what is required for three-dimensional simulation; a computer one third as large has been in operation at the Wright Air Development Center for seven years. There are two plugboards, which are removable, for each section of the computer, connections being made with shielded patch cords. The large amount of set-up-checking equipment is necessary, it was brought out, because even with a digital check solution available it is not possible to locate the causes of discrepancies, which merely generate hard feelings between digital and analog groups.

J. J. Gait of the Royal Aircraft Establishment, Farnborough, England, described another large machine, the "Tridac," which is intended for three-dimensional simulation at the R.A.E. and which will also be available to help British industry. It is ten times as large as the largest previous analog computer in the United Kingdom. The Tridac, which is even larger than the WADC machine, occupies two floors totaling 6,000 square feet of floor space, has 8,000 tubes, and consumes 650 kw. It was built by Elliott Brothers and has been in operation six months, though it still has a lot of bugs.

The Tridac contains two thousand manually set 0.1 per cent potentiometers, 6 electric and 9 hydraulic servos, and 600 operational amplifiers, of which 350 are stabilized by 400-cps mechanical choppers and 250 by magnetic modulators. The latter stabilizing system was experimental and doesn't work as well as the chopper stabilizer. Diode networks, nonlinear potentiometers, and cams are used to generate functions. The Tridac is composed of 2,000 "bricks" plugged into 44 cabinets, each brick being 12×8×3 inches.

Each of the 9 electronically controlled, hydraulically powered servos is driven by a 35-hp electric motor to pump oil at 2,000 psi. The natural frequency of these servos is 40 cps. They drive 224 potentiometers—some directly and some through sine and cosine linkages—and are used for axis transformation. Tridac simulation uses a synthetic 4-axis gimbal system and can take into account the varying mass of the plane, nonlinear aerodynamic coefficients, cross-coupling terms, etc.

Commercially Available Computers of Moderate Size

M. Gallo of Contraves A. G., Zurich, described his company's electromechanical ac (400 cps) analog computer. Its integrating element is a tachometer-generator, driven by an induction motor up to 180°. Each integrator drives a sine, a cosine, and six linear variable capacitors. The standard unit contains 12 adders and 18 integrators, which can be switched over to use as follow-up servos for multiplication. The components are made with 0.1 per cent accuracies. Computation times are generally kept under thirty seconds.

H. J. Uffler, Technical Director of the Calculator Department of the Cie. Générale de T.S.F., Paris, described his company's techniques for using high-frequency (500 kc) currents in analog computation for multiplication, addition, function generation, integration, and differentiation. These techniques are embodied in C.S.F.'s anti-aircraft fire-control computer KT 993, which measures 1.68×1.80×1.15 meters, weighs 1,450 kg, and uses 5 kva of 220-volt three-phase ac. The computing circuits are all balanced with respect to ground, and voltages of opposite phase represent positive and negative magnitudes.

The multiplier is a ladder network having three shunt inductances and, in each line, two series capacitances. Two additional capacitances are latticed across the first section of this network. The four capacitances in this first section are all formed with two concentric silvered steatite cylinders, cut so as to form eight hemicylindrical condenser plates. These condensers are driven by two-phase servo motors to obtain multiplication, function generation, integration, or differentiation, depending on how the motor is controlled. The motor rotor has a moment of inertia of 10 gm-cm² and can develop a torque of 1,000 gm-cm. The device becomes a resolver when the rotor plates are appropriately shaped. Addition is performed by shunting the inputs with inductances and connecting them through capacitances to a common inductance. The output appears across

another inductance which is capacitively coupled to this common inductance. The input and output impedances of these devices are claimed to be, for example, 500,000 ohms and 4 ohms, respectively. However, it would seem that such impedance ratios cannot be obtained without a compensatory 50-db drop in the voltage level. Precision of components is 0.1 per cent.

J. Armanville of the Société d'Électronique et d'Automatisme, Paris, described the S.E.A. analog computer type OME. L2 (Opérateur Mathématique Électronique), which has been available for two years. The computer contains, in a one-rack cabinet, 12 direct-coupled amplifiers, 18 hand-set potentiometers, 48 plug-in summation units, a removable patch-board, and test and maintenance elements. Several OME L2's can be joined together under the control of one of them; junction terminals are provided for this purpose at the sides of the patch-boards. Fundamentally, the OME L2 is intended for the solution of constant-coefficient linear differential equations, but plug-in units are available for the simulation of thresholds and saturation. Diode and servo multipliers and function generators can also be added. A special unit having additional potentiometers may be added for the solution of systems of up to 12 simultaneous linear algebraic equations.

J. Girerd of the Laboratoires Derveaux, Boulogne-sur-Seine, France, discussed his company's "Djinn" computer, which has the form of an office desk surmounted by six control panels in a convenient arrangement. The Dijnn has a removable patch-board, 40 potentiometers, and 30 plug-in amplifiers. The latter have a gain of 5×10^5 and a one-watt output at ±100 volts, input grid current being under 10^{-11} amp. The computer is intended only for linear, constant-coefficient problems, including inversion of tenth-order matrices.

H. Sokoloff of the Cie. Française Thomson-Houston, Groupe Électronique, Paris, described his company's equipment for plotting on two charts the path of an aircraft tracked by a COT/AL radar. One chart, oriented vertically, shows height as a function of rectangular coordinate, path length, or time, and the other, oriented horizontally, shows the plan of the path. The curve is interrupted at regular intervals of time. The plotter makes use of the radar range potentiometer and bearing and elevation resolvers to compute the rectangular coordinates and path length. Its accuracy is 0.1 per cent, its power consumption is 1.1 kw, and its price is twelve or thirteen million francs ($35,000).

Exhibition

An exhibition of analog computing equipment was held at 4, rue des Drapiers, in connection with the Analogy Computation Meeting. Among others, the foregoing five commercially available computers were on display. The C.S.F. fire-control computer, which is mounted in a truck trailer, was parked nearby in the avenue de la Toison d'Or. This van, known as type APT.HF 90, and said to be equivalent to the M9 computer, was built for the French Army and for U. S. offshore procurement under contract DA 91-557 EUC-169. It was open for public inspection.

The Société d'Électronique et d'Automatisme had on display its O.M.E. P2 computer, which is larger than the L2. The O.M.E. P2 contains three racks in cabinets, the racks being patched together by numerous short patch cords, and it has many small removable patchboards. Pictures were exhibited showing the Grand Simulateur de Vol, an extremely large flight simulator built by S.E.A. for the French government.

Short Bros. & Harland, Ltd., of Belfast, had on display their analog computer, which has the form of a desk with computing elements in and above the desk, its dimensions being $5\frac{1}{2}\times4\frac{1}{4}\times2\frac{1}{2}$ feet. A 4-inch double-beam cathode-ray tube with a 15-second persistence, a 1.5 per cent linearity, and a sweep time of 1/30 to 1 second displays one or two results against a time base or each other, and a single-pen recorder, occupying a desk drawer, records results on a 4-cm-wide chart. The recorder is good to 2 per cent up to 10 cps. On every other cycle of operation, drift corrections are automatically inserted.

The computer contains 18 five-tube amplifiers having a gain of 12,000, a maximum output of ±50 volts, an input grid current under 3×10^{-11} amp, and a cutoff frequency exceeding 15 kc; and 18 three-decade attenuators which also permit the selection of a multiplicative factor 0.1, 1, 10, or 100. The components are accurate to 1 per cent. The amplifiers and scaling units are plug-in packages of similar size, any five of which may be replaced by a quarter-square diode-network multiplier, a 21-segment diode-network function generator, or a "discontinuous-function generator," which is capable of simulating thresholds and saturation. The computer's power requirement is 1 kw; forced-air cooling is used. On its plug-board, which is not removable, only adjacent holes are joined.

The Elliott Brothers (London) G-PAC, a strictly linear analog computer costing £3,800 ($11,000) at the factory and occupying a cabinet $6\frac{1}{2}\times2\times2$ feet, was shown at the exhibition. The computer contains 20 amplifiers and 30 other components, as well as power supplies, a fan, a control panel, and a slow sweep for external cathode-ray display. The amplifier gain is 5×10^6 at dc and falls to 11,000 at 50 cps. Its maximum output is 1 watt at ±100 volts, the drift is less than 1 mv, the output ripple is under 12 mv, and the input grid current does not exceed 5×10^{-11} amp. Potentiometers are available with 2 per cent and 0.2 per cent precision. The computer components are packaged in small individual plug-in units, each having its own pin jacks; there is no patch board. Plug-in breadboards are available for the synthesis of functions, complex transfer functions, etc.

The computer requires 1.2 kva of 220 volts at 50 cps.

Information was available at the exhibition on Elliott Brothers' special cathode-ray crossed-field multiplier tube VCRX340, which has two perpendicular sets of deflecting plates, between which there is room to apply an axial magnetic field, and a pair of closely spaced, parallel "buckets" to collect the beam. The inputs are applied to the first pair of deflecting plates and the magnetic field, and the product, obtained from the buckets through a feedback loop, is applied to the second pair of deflecting plates to balance out the deflection caused by the magnetic field as a result of the transverse velocity imparted to the beam by the first pair of plates. A multiplier unit using this tube is designated K608. It measures $5\times16\times19$ inches. It is flat within 1 per cent and has a phase shift under 4° up to 1 kc. The response is down 1 per cent at 16 kc on one input and at 8 kc on the other. The maximum expected static error is under 0.5 per cent. Inputs and outputs range between ±50 volts. The unit requires external power supplies, including 4 volts at 1 amp and 1,400 volts at 0.4 ma.

Elliott Brothers displayed pictures of the Tridac and material concerning the AGWAC (Australian Guided-Weapons Analog Computer), which has been designed jointly by the British and Australian Ministries of Supply and Elliott Brothers, built by Elliott Brothers, and installed at the Long-Range Weapons Establishment, Salisbury, South Australia, for use in missile simulation. Its design is based on that of the Tridac, and many of its components are identical with those of the Tridac. The AGWAC is the largest computer in the southern hemisphere; it has 280 plug-in units $12\times8\times3$ inches which are fitted into 12 cabinets. An additional cabinet contains a small differential analyzer designed to handle a fourth-order system, and there is a control desk and a maintenance console. A closed-circuit refrigerated-air cooling system is used. The AGWAC uses diode networks for function generation, and it employs electromechanical multipliers and resolvers.

Other displays included: A Beckman Instrument Co., Berkeley Division, two-cabinet computer; a single-rack computer built by the Conservatoire des Arts et Métiers, Laboratoire National d'Essais, Paris; seven pictures of the various Westinghouse, Pittsburgh, computing facilities; pictures of the British National Physical Laboratory's Electronic Simulator, which contains six racks of mechanical computing elements servoconnected by means of a PBX-type patchboard; pictures of the Chalmers Institute of Technology's Electronic Integro-Differential Analyzer and of a number of its novel component developments; and pictures of the "Process Simulator," an analog computer built by the Koninklijke Shell Laboratorium in Delft, the Netherlands.

Conclusion

The technical sessions of the meeting were concluded with an announcement by F. H. Raymond of the decision by those who had chaired the sessions of the meeting to establish an International Association for Analog Computation (Association Internationale pour le Calcul Analogique) with permanent headquarters in Brussels. Professor M. J. Hoffman of the Université Libre de Bruxelles was elected president of the organizing committee. The organization is to publish a journal in which articles will in general appear in the author's language. The hope was expressed that similar organizations will be formed in the fields of digital computers and applied mathematics and that the several organizations may be united eventually into one.

The fifth day and last of the meeting, Saturday, October 1, was taken up with a visit to the computing facilities of the Université Libre de Bruxelles and an excursion to Bruges and Ghent.

Abstracts of all talks, in both English and French, were presented to the participants at the time of registration. The proceedings, including the complete texts of the talks and of the discussions, will be published.

On the basis of the exhibition and the papers presented at the meeting, it appears that France is America's nearest rival in the analog-computer field, followed closely by the United Kingdom, but good work is also being done in Sweden, Germany, Belgium, Italy, and Yugoslavia. The only paper presented at the meeting coming from the Soviet bloc concerned a simple analyzer for polynomials in Warsaw. However, the attendance at the meeting by four men from the U.S.S.R. Academy of Sciences in Moscow and one interpretress indicates an interest in this field on the part of the Soviet Union.

PGEC News

Announcement of Special Analog-Digital Issue for September, 1956

A special Analog-Digital issue of the Transactions on Electronic Computers is contemplated for September, 1956. The special issue is to be devoted to those papers which consider areas where computers of both the analog and the digital types are used together. R. D. McCoy, Reeves Instrument Corporation, 215 East 91 Street, New York 28, N. Y., is planning the issue and invites correspondence from authors. Authors are invited to send three copies of papers proposed for the issue to Mr. McCoy or the editor, R. E. Meagher, by May 1, 1956.

New Chapters Organized

Chapters of the Professional Group on Electronic Computers have been organized at Houston, Tex., and Montreal, Can. The total number of chapters is now fifteen. Copies of a directory, listing national and chapter officers and committee chairmen, are available from the editor of this column.

Meetings

Boston—A panel discussion on "Magnetic Storage Devices" was held at the November meeting. Panel members were J. A. Rajchman, RCA Laboratories; L. D. Stevens, IBM Research and Development Laboratory; W. N. Pappian, M.I.T. Lincoln Laboratory; R. C. Kelner, Laboratory for Electronics.

Dallas-Fort Worth—A tour of the Computing Laboratory at Convair served as the November meeting.

Akron—John Hosemann of the Clevite Research Center spoke on "Recording of Analog Signals" at the December meeting.

Philadelphia—H. Affel of Philco spoke on TRANSACS at the December meeting and R. L. Snyder discussed Magnistors at the January meeting.

Nominations Committee

The PGEC has appointed a Nominations Committee. The Committee consists of:

H. T. Larson, *Chairman*,
Ramo-Wooldridge Corp.,
8820 Bellanca Ave.
Los Angeles, Calif.

D. H. Gridley, *Vice-Chairman*,
Naval Research Lab.,
Washington, D. C.

C. W. Rosenthal,
Bell Telephone Labs.,
Whippany, N. J.

R. E. Meagher,
University of Illinois,
Urbana, Ill.

W. H. Ware,
The Rand Corp.
1700 Main St.,
Santa Monica, Calif.

The principal duties of the Committee are to make recommendations to the Administrative Committee of the areas from which the five new Administrative Committee members should come, notify pertinent chapter chairmen if nominations are to come from their areas, recommend nominations for PGEC Chairman and vice-Chairman and collect nominations for these posts from PGEC members.

IRE National Convention

Electronic Computers I—Wednesday, March 21, 10:00 A.M. to 12:30 P.M. in Marconi Hall.

Session Chairman. D. R. Brown, M.I.T. Lincoln Laboratory.

1. *A Multiple Input Analog Multiplier*, by D. D. Porter and A. S. Robinson, Columbia University.
2. *Analogue Multiplying Circuits Using Switching Transistors*, by Kan Chen and R. O. Decker, Westinghouse Electric Corporation.
3. *Characteristics of the RCA BIZMAC Computer*, by A. D. Beard, L. S. Bensky, D. L. Nettleton, and G. E. Poorte, RCA.
4. *Input and Output Devices in the RCA BIZMAC System*, J. A. Brustman, K. L. Chien, C. T. Cole, Jr., and D. Flechtner, RCA.
5. *The Burroughs Series G High Speed Printer*, E. M. DiGiulio, Control Instrument Company.

Electronic Computers II—*Wednesday*, March 21, 2:30 P.M. to 5:00 P.M. in Marconi Hall.

Session Chairman: J. H. Howard, Burroughs Research Center.

1. *A Magnetic Drum Sorting System*, by B. Cox and J. Goldberg, Stanford Research Institute.
2. *A Magnetic Drum Extension to the Gamma 3 Computer*, by P. L. Dreyfus, H. G. Feissal, and B. M. Leclerc, Compagnie Des Machines Bulletin.
3. *The Univac Magnetic Computer, Part I—Logical Design and Specifications*, A. J. Gehring, L. W. Stowe, and L. W. Wilson, Remington Rand Univac.
4. *The Univac Magnetic Computer, Part II—Megacycle Magnetic Modules*, B. K. Smith, Remington Rand Univac.
5. *The Univac Magnetic Computer, Part III—Drum Memory*, V. J. Porter, S. E. Smith, and M. Naiman, Remington Rand Univac.

Symposium—Thursday, March 22, 10:00 A.M. to 12:30 P.M. at Waldorf-Astoria Hotel.

Impact of Computers on Science and Society

International Meeting on Automation

An international meeting and exposition on automation is planned to be held in Paris on June 18–24, 1956. It is anticipated that papers will be presented on automation from the theoretical, experimental, engineering, and production points of view. Correspondence pertaining to the proposed meeting should be addressed to

Secrétariat du Colloque sur l'Automatique,
Chaire de Mécanique,
Conservatoire National des Artes et Métiers
292 rue Saint-Martin
Paris (III°), France.

Stanley B. Disson
News Editor
Burroughs Research Center,
Paoli, Pa.

Review of Electronic Computer Progress During 1955

J. P. NASH†

Introduction

A FEW YEARS AGO when one wanted to sit down quietly at the end of a year and reflect upon the advances made in the field of electronic computers he found it a not very complicated process. The chances were good that he knew someone in nearly every organization that was contributing to the field and that he needed only to run over in his mind the groups of people who were doing computer work. If his interest lay in digital computers, he could name every operating digital computer in the world and could probably recite its characteristics.

Today all this has changed. It is not even possible to say with certainty who is or who is not doing work in the computer field. With the engineers who design and build computers taking advantage of every new product of the research laboratories, results arising in physics or chemistry may turn out to have significant applications in the development of computer components. Contributions are published in such a wide variety of different journals that in a day's browsing through only the electrical engineering journals of one year to be found in a large library one can find literally hundreds of articles which are specifically concerned with analog and digital computers. Most of the contributions come from the United States and from England, but the reader can readily find articles from Australia, Japan, France, Italy, Germany, Sweden, and other countries. And of course progress in the field of electronic computers is not confined to the computers themselves. Very important advances are being made in the use of machines, especially in fields more remote from those in which computers first found application—fields including the social and management sciences and the enormously great applications in business operations. Articles on these topics will be found in a vast multitude of other journals and publications.

Perhaps the characteristic most evident in the year 1955 was volume. We have entered the production phase of computers, especially digital computers, and in 1955 there appeared from more than a dozen manufacturers a greater number of general purpose digital computers than had previously been built up to 1955. Most of these were medium-speed machines using magnetic drums as storage devices. Much of the emphasis by the manufacturers was upon the advantages of these computers for business applications [109], for it is in the business world that the mass market for computers lies.

† Digital Computer Laboratory, Univ. of Illinois, Urbana, Ill.

In addition to large installations in such companies as General Motors, General Electric, DuPont and many life insurance companies, a great many companies are setting up small computing establishments.

Systems

The new computers announced or beginning to appear in 1955 showed an even wider spread in cost and complexity than ever before, ranging in price from about $60,000 for some of the smaller medium-speed machines to the multimillion dollar level for special one-of-a-kind computers. Many of the smaller machines have features [1] such as index registers, multiple-precision operations, floating point operations, decimal operations, and automatic number conversion which make them as versatile as the larger computers; the principal difference is in speed.

The fastest scientific computer yet proposed was announced by the Sperry Rand Corporation. To be known as the LARC, the machine will be built for the Livermore Laboratory of the Atomic Energy Commission, delivery to be in 1958. It will be a decimal machine using transistors, magnetic amplifiers, and printed circuits. The internal memory will consist of 8 units of 2,500 words each, using magnetic cores, while magnetic drums will increase the total memory capacity to 96,000 words. There will be 100 index registers. Addition and multiplication will require 4 and 8 microseconds, respectively, while division is expected to take 28 microseconds. The size of the machine may be estimated from the predicted numbers of components: transistors, 5,000 to 8,000; diodes, 25,000 to 74,000; magnetic amplifier units, 10,000 to 16,000.

A large system specifically created to handle business problems, the BIZMAC, was announced by the Radio Corporation of America. The basic computer utilizes a three-address instruction in octal notation. There is a 20 microsecond access core memory of 2,048 or 4,096 characters, a drum memory for program storage, and elaborate magnetic tape facilities for handling from a few to a few hundred tapes. Input is by paper tape or transcribed IBM card; output is by a high-speed electro-mechanical printer or electronic printer.

A number of systems have made use of solid state devices or have adopted printed circuit techniques. North American Aviation Corporation has built for the Air Force a 125 pound airborne digital computer using 1,000 transistors and printed circuits. Contained in three cubic feet of space, it requires less than 100 watts of power. The Bendix G-15 general purpose computer and D-12 digital differential analyzer are assembled

from printed-circuit packages. The TRANSAC built by the Philco Corporation for airborne use has an arithmetic unit which contains 1,242 surface barrier transistors and which uses less than 6 watts of power.

Components

Research in computer components has been heavy in transistors and magnetic cores. In this connection it is interesting to recall some remarks made six years ago by L. N. Ridenour:[1] "Probably there is no more rewarding direction for computer development than to explore the possibilities of using unconventional elements in the design of such machines. If the vacuum tube can be replaced with a cheaper, simpler, and more durable device, then the over-all competence of practicable computers can be greatly increased. Such a development will bring in its train a greater availability for computers of the present sort, and a wider general use of computing machines of all kinds."

Memory Components

The ferromagnetic core [14, 18, 19, 21] has received the most emphasis as a memory device and results obtained with magnetic cores have been very satisfying. In February 1955, a large magnetic core memory (4,096 40-bit words) was delivered by International Telemeter to the RAND Corporation of Santa Monica, California. During its first six months of operation this memory made only 18 errors in 1,070 hours of computing time. Much larger memories than this have been announced by International Telemeter, which expects to complete in 1956 a memory with more than 110,000 bits per digit plane and by IBM which has announced the forthcoming availability of a 32,768 word memory with a random access time of 12 microseconds for its Type 704 computer. The UNIVAC and UNIVAC SCIENTIFIC computers of Sperry Rand are also being provided with core memories. Various different techniques for using cores in groups [31] and for designing memories having very fast read out [22] have also been proposed.

Memory work has continued in electrostatic techniques [28, 29] and in magnetic drum recording methods [26, 27, 32]. A new memory device utilizes an electro-optical feedback circuit [30]. Two other phenomena which have been studied for possible use as memory components are the actions of ferro-electric materials such as barium titanate [17, 23] and the characteristics of nuclear resonances [24, 25]. Neither of these has reached the state of development of ferromagnetic devices.

Circuit Components

A great deal of attention has been concentrated upon the design of transistor circuits [33, 36, 41, 45, 47] with the aim of producing flip-flop and gate circuits which will operate in the millimicrosecond range [46]. The most important single contribution to this has probably been the production by the Philco Corporation of a surface barrier transistor having an α-cutoff of 60 megacycles per second. These transistors have made possible the design of fast and yet simple direct-coupled circuits [49].

Magnetic cores as circuit elements have also received a considerable amount of attention [34, 35, 38, 50].

IBM has announced a new transistor with thyratron-like characteristics which is capable of switching current loads of approximately 100 milliamperes at pulse rates of one megacycle per second. When operated at maximum ratings it can switch power loads of about 5 watts and is expected to be useful in core-switching applications.

Input-Output Components

High-speed printers have been appearing in greater numbers. The IBM Corporation has announced a fast printer, and the Sperry Rand Corporation has on the market [51] a printer capable of producing 1,000 characters per second in lines up to 130 columns wide. A direct display storage tube, the Typotron [52], built by Hughes Aircraft Company can display a character in 40 microseconds and hold it until it is erased. The electrographic recording method [53] of the Burroughs Corporation utilizes a controlled source of charge to form small charged areas on coated paper. Characters formed from a 5 by 7 matrix can be recorded at rates exceeding 5,000 characters per second.

Logical Design and Switching Theory

The recent results in faster circuits have encouraged further efforts to produce more efficient logical design of arithmetic components. New work has been done in the design of counters [59, 64, 65, 68], scalers [67], adders [56], and multipliers [75]. There have also been new results in switching theory [61, 62, 72], in the application of Boolean methods to the analysis and synthesis of circuits [70, 71, 73], and in the theory of logical nets [74].

Control, Simulation and Non-Numerical Use

Analog computers have long been and still are foremost in most simulation [84, 85] and real time problems, but work is being done toward the use of digital machines in such problems [78, 79, 86] and more useful results will certainly be achieved as machine speeds are increased. A considerable amount of work is also being done in the study of learning processes and pattern recognition by digital methods [80, 81, 82, 83].

Analog Computation

The formal computer literature contains much more material on digital computers than it does on analog computers. This is unquestionably due to some extent

[1] L. N. Ridenour, "High speed digital computers, an elementary survey of present developments and future trends," *J. Appl. Physics*, vol. 21, pp. 263–270; April, 1950.

to the fact that, as special purpose devices, the analog machines or components are reported upon in journals which are concerned more with the equipment of which the computer forms a part than with the computer itself. Therefore a true picture of the year's results in analog computers can be obtained only by the reviewing of a prohibitively large amount of literature. In analog components there has been further research in amplifiers [87, 95], multipliers [98], network synthesis [89, 90], and function generators [100, 101]. Descriptions have been given of a number of special computers for automatizing network analyzers [91], calculating tristimulus color values [92], and solving linear equations [97].

Use of Machines

No review would be complete without some remarks about the use of machines, and yet the uses to which analog and digital computers are put, even the new uses, are much too great in number to allow any conscientious listing. Little more has been done in the references listed at the end of this article than to indicate uses which may interest the usual readers of this journal. Special attention should be called to a survey of analog computer installations [106], to a comprehensive examination of digital computers and their characteristics [109], and to the results of a conference on training personnel for the computer field [124].

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Reviews of Current Literature

It is the intention of this section to review articles that have been published since January 1, 1953, and to publish eventually reviews of all books pertaining to the computer field. Authors can be of considerable assistance in this review process by sending two reprints of their articles to H. D. Huskey, Department of Electrical Engineering, University of California, Berkeley, California. The editors wish to express their gratitude to the reviewers who, through their efforts, make this section possible.

H. D. Huskey, Editor

GENERAL

56-1

Will Electronic Principles Make Possible a Business Revolution?—W. W. McDowell. (*Trends in Computers: Automatic Control and Data Processing, Proc. Western Computer Conf., Joint AIEE-IRE-ACM, February 1–12, 1954, Los Angeles, Calif.*, pp. 9–15; April, 1954.) The author points out that, although most of the present business computers have been developed to perform automatically exactly those clerical operations now occupying the business world, there is every reason to suppose that still greater savings are possible by a new approach to the problem. The attack which he then goes on to explore is one of a scientific analysis of business operations, needed, he feels, so that better systems of data processing may be designed in which computers are a well integrated part. There is, therefore, need for the introduction of persons who might be called business research engineers into the field of business systems analysis. The scientific approach to the problems of the business world will meet tasks more difficult than those encountered in developing the automobile production line, for instance. The rewards, however, will also be greater. Mr. McDowell acknowledges that the mounting of such an attack on business problems on the scale necessary will be costly. He believes, nevertheless, that if business management can be convinced of the merit of this approach the money will be found to carry out the job.

Oliver Whitby

56-2

Publications for Business on Automatic Computers: A Basic Listing—Ned Chapin. (*Computers and Automation*, vol. 4, pp. 13–16, 38; September, 1955.) Publications about computers and computer applications which are written in a language which can be understood by the businessman are listed in this bibliography.

G. Morrison

56-3

Who Are Manning the New Computers?—John M. Breen. (*Computers and Automation*, vol. 4, pp. 28, 36; October, 1955.) While it was initially expected that the operating personnel of large computers would have to be highly skilled specialists, the author feels that, in practice, most organizations are

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—The Editor

training their own employees and getting better results than if specialists had been used. He expects that the users of this equipment will eventually have to go to the specialists to improve the efficiency of their operations. However, no statistics are presented to verify the author's observations or his expectations.

G. Morrison

56.4

A Diode Multiplexer for Analog Voltages—H. J. Gray, Jr., M. Rubinoff, and J. Tompkins. (*Trans. IRE*, vol. EC-4, pp. 64–66; June, 1955.) The article describes a diode multiplexing switch for analog voltages which is of particular interest in connection with analog-to-digital converters. The complexity and cost of high-sampling-rate electronic conversion equipment very often demands that a large number of analog voltages be sampled by a single converter or, conversely, that the analog output of a converter be distributed to many points. A fast, accurate switch therefore, is desirable. The described device fulfills, to a degree, these requirements. The accuracy is within 1 per cent of full scale (full scale being ± 5 volts) and the switching time is of the order of 100 μs. The limits of operation are confirmed by both theoretical equations and experimental results. Operation with commercially available silicon junction diodes, both matched and unmatched, is evaluated.

George J. Giel

56.5

A Transistorized Pulse Code Modulator—G. R. Partridge. (*Trans. IRE*, vol. EC-3, pp. 7–12; December, 1954.) This paper describes a method of converting an analog signal to a digital representation. The conversion is accomplished in three steps: 1) Relate the analog signal to the closest discrete voltage level. (a) For an n binary bit system, there are 2^n discrete levels. (b) This part of the circuit utilizes $2^{n+1}-3$ reference voltages (batteries), 2^n-1 diodes, 2^n-1 transistor amplifiers, and passive elements in the form of resistors and diodes. (c) At a point of transition between two voltage levels, the "play" in the circuit is adjustable from the point where the circuit will choose neither voltage level to the point where the circuit will choose both voltage levels. 2) Generate a "parallel" digital representation of the voltage level chosen in step 1) by use of a diode matrix. (a) Output may be Gray code or Straight Binary. (b) The author suggests adjusting the "play" (1c) for a moderate amount of overlap and the choice of the Gray code as a means of providing a non-ambiguous conversion system. 3) Convert the "parallel" digital representation to a "serial" digital output by a circuit which utilizes transistors, diodes, and passive elements. The system will encode inputs at the rate of 5,000 per second.

Saul Meyer

56-6

Minimizing and Mapping Sequential Circuits—W. S. Bennett. (*Commun. and Elec.*, no. 20, pp. 443–447; September, 1955.) A map method is described for developing circuits of the sequential type which contain a minimum number of components. The map is similar to one used previously by Karnaugh for nonsequential circuits except that some points of the map represent storage or memory of previous conditions. Convenient use of the map is limited to circuits with four or fewer relays and the scheme has not yet been extended to selector switches, steppers, and latching relays. Two examples are worked out in detail. One is a circuit which responds to two signals in accordance with which arrives first, and the other is a relay flip-flop. Although the paper is a contribution to an important and difficult subject, it seems more to point up the problems involved in designing sequential circuits than to provide a method whereby circuits generally encountered in practice may be designed.

R. K. Richards

ANALOG COMPONENT RESEARCH

681.142 56-7

Gating Multipliers—M. Lilamand. (*Onde Elect.*, vol. 35, pp. 142–150; February, 1955.) Analog computing equipment on lines proposed by Goldberg (Abstract 151, *Proc. IRE*, February, 1953) is described. Economy of materials is achieved by careful design of the switching circuit and by neutralization of the parasitic capacitances of the tubes. An accuracy to within one part in 1,000 at a mean gating frequency of 1.5 kc is obtained.

Courtesy of Proc. IRE and *Wireless Engineer*

ANALOG EQUIPMENT

681.142:512 56-8

Linear Algebraic Computation by Multiwinding Transformers—F. L. Ryder. (*J. Franklin Inst.*, vol. 259, pp. 427–439; May, 1955.) Theory is presented of transformer circuits for solving simultaneous equations and inequalities; the reduction of errors due to transformer imperfections is discussed. The practical aspects are illustrated by a problem involving checking the compatibility of ten inequalities with six variables. The present device is similar to that described by Mallock (*Proc. Roy. Soc. A*, vol. 140, pp. 457–483; May, 1933).

Courtesy of Proc. IRE and *Wireless Engineer*

681.142:621.37 56-9

The Solution of Plane Stress Problems by an Electrical Analogue Method—G. Liebmann. (*Brit. J. Appl. Phys.*, vol. 6, pp. 145–157; May, 1955.) "It is shown that the biharmonic equation $\nabla^4\chi=0$, which Airy's stress function has to satisfy, can be solved by an electrical analogue comprising two resistance networks in cascade."

Courtesy of Proc. IRE and *Wireless Engineer*

621.384.622:681.142 56-10

A Computer for Solving some Problems in Connection with Travelling-Wave Particle Accelerators—M. C. Crowley-Milling. (*Metrop. Vick. Gaz.*, vol. 26, pp. 127–131; April, 1955.) A mechanical system is described comprising a motor generator which, in conjunction with an amplifier and feedback system, is arranged to have an angular velocity proportional to the translational velocity of the particles.

Courtesy of Proc. IRE and *Wireless Engineer*

56-11

A Dependent Variable Analog Function Generator—C. J. Savant, Jr. and R. C. Howard. (*Proc. WESCON Computer Sessions, August 25–27, 1954, Los Angeles, Calif.*, pp. 2–12; 1955.) This article describes an all electronic nonlinear function generator. A linear function is converted to a logarithmic function by using the logarithmic relationship of grid current to plate current in a vacuum tube. By using a combination of these converters and their inverse, the article discusses how various nonlinear functions may be generated. Block diagrams of typical functions, schematics of the generator, together with the resulting accuracies, are given in the article. It is an interesting and useful device for producing nonlinear functions at high or low speeds and with control over the characteristic of the nonlinear function.

J. B. Speller

56-12

Correlation Computation on Analog Devices—V. S. Haneman and J. W. Senders. (*Jour. Assoc. Comp. Mach.*, vol. 2, pp. 267–279; October, 1955.) The correlation function in general form is

$$\phi(\tau) = \lim_{T\to\infty} \frac{1}{2T}\int_{-T}^{T} f(t)g(t+\tau)dt$$

Its application to communication theory has gained considerable importance in the past few years; *e.g.*, 1) filtering, 2) prediction, 3) statistical analysis, etc. For this reason a number of special purpose computers have been constructed to facilitate its computations. This article gives the names, with brief description and comments, of the laboratories and institutions which have correlation computers. [For electrical engineers who would like to have a basic knowledge of correlation analysis, the reviewer recommends the following: "Principles of Statistical Analysis," *Automatic Feedback Control System Synthesis*—John G. Truxal, ch. 7, (McGraw-Hill, New York; 1955); see 56-52, this issue.]

J. C. Chu

UTILIZATION OF ANALOG EQUIPMENT

56-13

Solution of Linear Differential Equations with Variable Coefficients by the Electronic Differential Analyzer—Carl E. Howe and Robert M. Howe, (Trans. IRE, vol. EC-2, pp. 3–8; December, 1953.) The article is divided essentially into three parts. The first part describes a novel arbitrary function generator using relays to switch resistors. The device as described was built to provide a resistance whose value may change in a step-wise manner as any predetermined function of time. The resistance change is accomplished by means of a stepping switch, toggle switches, and binary resistors. The stepping switch selects the rows of toggle switches one at a time uniformly with time. The toggle switches are preset to short out

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combinations of the binary resistors such that essentially any value of resistance may be so switched in. Accordingly, the device can be used to provide an accurately controllable variable resistance element for use with an electronic analog computer to solve partial differential equations. The second part describes the use of this time varying resistance element for the solution of linear differential equations with time varying coefficients. The example chosen is Bessel's equation. Differential analyzer solutions are compared to theoretical solutions, showing accuracies of the order of 1 to 0.1 per cent are attainable. The third part describes a method for setting the time constant of an integrating amplifier. The technique uses a 3-amplifier oscillator circuit to determine accurately the values of the integrating capacitors. The resistors are then matched to the value of the capacitor. Accuracies of the order of 0.01 per cent are said to be attainable.

Joseph L. Hussey

DIGITAL COMPONENT RESEARCH

681.142 56-14

Storage Devices for High Speed Calculators—A. D. Booth. (*Research* (London), vol. 8, pp. 130–140; April, 1955.) A survey covering thermal, optical, sonic-delay, electrochemical, cr tube, ferroelectric, capacitor, magnetic-drum, magnetostriction, and magnetic-core devices.

Courtesy of PROC. IRE and *Wireless Engineer*

56-15

A Multistable Transistor Circuit—R. A. Henle. (*Commun. and Elec.*, No. 21, pp. 568–571; November, 1955.) Several different variations of a multistable transistor circuit are described. A multiplicity of stable states is achieved by using a step-like load line in a circuit containing feedback. The step-like load line can be realized either through a set of diodes connected to a series of different supply voltages in a special circuit or by using a number of Zener diodes. The preferred feedback circuit is composed of two junction transistors, one connected in grounded-base fashion and the other as an emitter follower. Other circuits are possible, including a single-transistor arrangement where the transistor has an alpha greater than unity. Circuits are shown for causing the multi-stable configuration to step from one state to the next.

R. K. Richards

621.318.57:621.314.7 56-16

Directly Coupled Transistor Circuits—R. H. Beter, W. E. Bradley, R. B. Brown and M. Rubinoff. (*Electronics*, vol. 28; pp. 132–136; June, 1955.) The characteristics of surface barrier and certain alloy-junction transistors permit the design of computer circuits with direct coupling between stages. By taking advantage of this design the number of resistors and condensers required can be reduced considerably. Response of these units is also very good. The surface barrier transistor used in two-state operation offers state-to-state transition in a tenth of a microsecond or less. This article describes a set of high speed computer circuits using surface barrier or alloy-junction transistors. Typical circuits for flip-flops, "and" circuits, "or" circuits and delay univibrators are discussed. A complete half-adder circuit is shown indicating the simplicity which may be obtained by using these transistors and circuit techniques. These circuits employ grounded-emitter operation with direct coupling between the collector of one stage and the base of succeeding stages.

Norman F. Loretz

621.374.32:621.318.57 56-17

Nonsaturating Pulse Circuits Using Two Junction Transistors—J. G. Linvill. (PROC. IRE, vol. 43, pp. 826–834; July, 1955.) Junction transistors are found to be fast enough for pulse applications if the collector voltage is prevented from reaching zero. Switching times $<1\ \mu s$ can be achieved with available types. The required limiting action is effected by introducing diodes which terminate the switching transients by their breakdown. A two-transistor binary counter is described.

Courtesy of PROC. IRE and *Wireless Engineer*

681.142:621.395.625.3 56-18

Magnetic Recording Applied to (digital) Computers—F. H. Raymond. (*Onde Élect.*, vol. 35, pp. 89–96; February, 1955.) The basic considerations involved in the design of the magnetic storage drum used in the C.U.B.A. machine are discussed. Optimum dimensions of pole faces for recording and reproducing heads are calculated and design curves are given.

Courtesy of PROC. IRE and *Wireless Engineer*

538.221:681.142 56-19

Magnetic Materials for Digital-Computer Components: Part 2—Magnetic Characteristics of Ultra-thin Molybdenum-Permalloy Cores—N. Menyuk. (*J. Appl. Phys.*, vol. 26, pp. 692–697; June, 1955.) Observations of the flux-reversal characteristics were made for tapes of various thicknesses at seven temperatures in the range -196 to $+270$ degrees C. The results indicate that the eddy-current contribution to the switching delay falls by about 50 per cent and the spin-relaxation contribution by about 20 per cent between the lower and upper ends of the temperature range. This behavior gives support to the theory presented in part 1 by Menyuk and Goodenough (Abstract 1713, PROC. IRE, July, 1955).

Courtesy PROC. IRE and *Wireless Engineer*

681.142:538.221 56-20

Multiple-Coincidence Magnetic Storage Systems—R. C. Minnick and R. L. Ashenhurst. (*Jour. Appl. Phys.*, vol. 26, pp. 575–579; May, 1955.) "In existing magnetic matrix storage systems a given location is selected by applying to two intersecting wires a current equivalent to one-half of the selecting field. This situation is generalized so that any core is selected by energizing p wires each with a current equivalent to $1/p$ of the selecting field. The advantages gained are in the correspondingly smaller fields applied to the nonselected cores, or alternatively, in the faster switching times obtainable by applying a total field greater than the coercive force to the selected core. . . . Specifically, a storage matrix is illustrated in which the cores are toroids etched from a continuous sheet of magnetic material."

Courtesy of PROC. IRE and *Wireless Engineer*

538.221:621.318.134 56-21

A Note on the Rectangular Magnetization Loop of Ferrite Cores—M. Kornetzki. (*Frequenz*, vol. 9, pp. 81–83; March, 1955.) It is pointed out that the so-called rectangular loops of commercially available Mg-Mn-ferrite cores are not rectangular in the strict sense applicable to the loops of oriented-structure magnetic metals. The remanence value of 0.9 is obtained only for weak applied fields up to a few oersted, and falls to about 0.6 if the remanent magnetization is related to the true strong-field saturation magnetization. The low slope of the upper and lower branches of the loop is probably due to high crystal energy and sudden initiation of irreversible inversion of magnetization at a field strength near the coercive force.

Courtesy PROC. IRE and *Wireless Engineer*

56-22

Magnetic Amplifiers in Bistable Operation—L. A. Finzi and G. C. Feth. (*Commun. and Elec.*, No. 21, pp. 592–598; November, 1955.) The paper is a general discussion of the factors affecting bistable or flip-flop action of magnetic amplifiers. No new circuits or applications are presented.

R. K. Richards

538.221:621.318.134 56-23

Relaxation Phenomena in Ferrites—A. M. Clogston. (*Bell. Syst. Tech. J.*, vol. 34, pp. 739–760; July, 1955.) The mechanism suggested *e.g.* by Galt *et al.* (Abstract 2446, PROC. IRE; September, 1954) for the losses observed in ferromagnetic resonance and domain-wall motion in single crystals of Ni ferrite containing small amounts of divalent Fe is critically discussed. Expressions for the velocity of domain-wall motion, for the line width in ferromagnetic resonance and for the displacement of the field for resonance are deduced from a theory based on a thermodynamic model.

Courtesy of PROC. IRE and *Wireless Engineer*

621.318.5 56-24

Parallel-Ferroresonant Feedback-Type Trigger Circuit—J. G. Santesmases and M. R. Vidal. (*Onde Élect.*, vol. 35, pp. 165–173; February, 1955.) A self-excited circuit consisting of an ac winding on a ferromagnetic core, shunted by a capacitance, with auxiliary windings for excitation and polarization, may be adjusted to present two, and in certain conditions, three, stable states. Curves are given showing the influence of the various parameters.

Courtesy of PROC. IRE and *Wireless Engineer*

621.318.5 56-25

A Shifting Register Using Ferroresonant Flip-Flops—S. Duinker. (*Appl. Sci. Res.*, vol. 4B, pp. 317–328; 1955.) An arrangement is described in which the information can be shifted in either direction, depending on the

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rity of the shifting pulse. Consideration iven to design for operation with supply quencies in the mc range.

Courtesy of PROC. IRE and *Wireless Engineer*

.227 56-26

New Class of Ferroelectrics—A. N. lden, B. T. Matthias, W. J. Merz, and P. Remeika. (*Phys. Rev.*, vol. 98, p. 546; ril 15, 1955.) Guanidine aluminium sul- te hexahydrate $(CN_3H_6)Al(SO_4)_2.6H_2O$ been observed to be ferroelectric at nperatures from about 200 degrees C vnwards.

Courtesy of PROC. IRE and *Wireless Engineer*

.227:546.431.824-31 56-27

Etch Patterns and Ferroelectric Domains $BaTiO_3$ Single Crystals—J. A. Hooton l W. J. Merz. (*Phys. Rev.*, vol. 98, pp. -413; April 15, 1955.) Technique for in- tigating ferroelectric domains in $BaTiO_3$ based on the observed fact that the posi- e end of the electric dipole in the material hes much faster than the negative end.

Courtesy of PROC. IRE and *Wireless Engineer*

.227./228:537.311.33 56-28

Space-Charge Layer Near the Surface of erro-electric——W. Känzig. (*Phys. Ref.*, . 98, pp. 549–550; April 15, 1955.) eoretical considerations indicate that ce-charge layers and associated strong ctric fields near the surface of highly arizable semiconductors could produce ervable piezoelectric or electrostrictive ain. Experimental evidence for the exist- e of such layers in $BaTiO_3$ is mentioned.

Courtesy of PROC. IRE and *Wireless Engineer*

.227:546.431.824-31 56-29

Dynamic Behavior of Domain Walls in rium Titanate—E. A. Little. (*Phys. Rev.*, . 98, pp. 978–984; May 15, 1955.) nematographic technique was used to dy domain nucleation and subsequent ll movements in $BaTiO_3$ single crystals, ulting from application of direct, alternat- or pulse voltages up to 500 v. Photo- phs and diagrams illustrate the processes served.

Courtesy of PROC. IRE and *Wireless Engineer*

.318.57:546.289:535.215 56-30

A Two-State Light-Activated Circuit Ele- nt Using Germanium—J. W. Granville. *rit. J. Appl. Phys.*, vol. 6, pp. 172–173; y, 1955.) A bar of *n* type germanium h a potential difference across its ends l a suitably biased point contact near the ldle will show double-base-diode action. e point-contact diode will conduct, or se to conduct, according as one end or the er of the bar is illuminated, both sides ng stable when the light is removed. In ctice the bar is divided near the point tact and the two parts are connected copper wire to ensure that holes gen- ted in one section recombine before they swept into the other.

Courtesy of PROC. IRE and *Wireless Engineer*

56-31

Engineering Multistage Diode Logic Circuits—B. J. Yokelson and W. Ulrich. (*Commun. and Elec.*, No. 20, pp. 466–475; September, 1955.) Various design considerations for diode "and" and "or" circuits are presented where there may be up to three levels or stages of logic. The considerations for the most part under the assumptions that transistor circuits will be the driving sources and the output loads. Several special techniques are described involving logic branching, partial relay logic, and condenser coupling.

R. K. Richards

621.373.431.1 56-32

Analysis of the Relaxation Period of a Multivibrator—D. C. Sarkar and R. Ahmed. (*Indian J. Phys.*, vol. 28, pp. 533–541; November, 1954.) The analysis takes account of positive grid swing and appreciable shunting capacitance. Comparison of values obtained from the theory with experimental results indicates that the method is satisfactory.

Courtesy of PROC. IRE and *Wireless Engineer*

56-33

Design Fundamentals of Photographic Data Storage—Gerhard L. Hollander. (*Proc. WESCON Computer Sessions, August 25–27, 1954, Los Angeles, Calif.*, pp. 44–49; 1955.) An evaluation of photographic emulsions as medium for storing digital information requires design parameters not generally available. This paper discusses what is required to design the recording equipment, and to estimate errors. The reading problem is touched upon.

G. W. King

56-34

Binary Adder Tube for High-speed Computers—F. B. Maynard. (*Electronics*, vol. 28; pp. 161–163; September, 1955.) A binary adder tube for high-speed computers is described in this article. This single tube plus a few external components performs all the functions capable of more complicated multiple tube circuits usually used to build up a binary adder. Fast operational speeds are obtained and the carry output from one tube is able to drive a following tube without additional amplification. The author states the speed of a single tube when used as a serial adder is in the region of one megacycle. However, in parallel adder applications the maximum operational speed decreases as the number of adder stages increases. A four stage adder is described with operation at pulse rates up to 100 kc. Applications other than straight binary addition are also described.

Norman F. Loretz

DIGITAL EQUIPMENT

56-35

Synchronizing Magnetic Drum Storage Speed—E. W. Bivans. (*Electronics*, vol. 28; pp. 140–141; August, 1955.) A method of synchronizing a magnetic drum storage system to an acoustic delay-line storage system is described. The drum uses circulating channels which have a time delay equal to that of the acoustic delay line. Synchronization is accomplished by using an error signal, derived from the two supposedly in phase clock signals, to control the drum motor speed. By comparing a proper amount of the error signal against a known voltage the involved servo system can bring the error to zero. With plus or minus ten per cent changes in line voltage or plus or minus three per cent variation in acoustic delay-line sync pulse frequency a synchronizing accuracy of plus or minus one-half microsecond is obtained.

Norman F. Loretz

681.142 56-36

Electronic Computers for the Businessman—J. M. Carroll. (*Electronics*, vol. 28; pp. 122–131; June, 1955.) This article is sure to be of great interest to all who are concerned with computers for business. It is a survey of the characteristics of thirty-eight modern computers. In the text the author gives a general description of many computers. He also briefly describes the operation of some storage systems and input-output devices. A great deal of information is supplied in table form. Table I gives such information as cost, availability, power consumption, space requirements, and operating personnel required for thirty-eight computers. Table II lists technical characteristics and operation capabilities. Table III shows methods and characteristics of the storage devices of thirty-two computers. Table IV lists the type and speed of input-output systems, and Table V gives operating speeds of these computers.

Norman F. Loretz

56-37

The Bendix G-15 General Purpose Computer—Harry D. Huskey and David C. Evans. (*Proc. WESCON Computer Sessions, August 25–27, 1954, Los Angeles, Calif.*, pp. 87–91; 1955.) A description of the logical, electronic, and physical characteristics of the Bendix Model G-15 general purpose computer. The G-15 is a stored program magnetic drum computer with a memory of over 2,000 words. Quick-access loops are provided to increase computational speed. The command structure is quite flexible, so that single or double precision operations, or an entire block transfer, can be accomplished with a single command. The standard input-output equipment consists of a photoelectric tape reader, a tape punch, and an electric typewriter. Magnetic tape and circuits to accommodate punched card equipment are also available. Input-output operations are buffered so that computation may proceed during these operations. The G-15 is constructed in a single cabinet $27'' \times 30'' \times 60''$ high. Two swing-out gates contain all of the electronic circuitry on plug-in printed circuit cards. Power consumption is about 3 kw, and forced-air cooling is employed.

Vernon C. Kamm

56-38

An Experimental Transistorized Calculator—G. D. Bruce and J. C. Logue. (*Elec. Eng.*, vol. 74, pp. 1044–1048; December,

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55.) This article describes the transis-ized version of the IBM 604 Electronic lculating Punch. A brief system descrip-n is given. Most of the article is devoted circuit description. The following circuits e described, including diagrams: inverter, itter follower, trigger, decimal counter, ing ring, logical circuits, and output ver. p-n-p and n-p-n germanium junction nsistors are used, with 1 mc alpha cutoff d a grounded emitter current gain of 40 nimum and 90 maximum. The machine es 2,165 transistors and 3,600 germanium odes, with no vacuum tubes. The machine es 310 watts, about 5 per cent of the power quired by the vacuum tube version of the 4.

Harry T. Larson

1.142 56-39

A Proposed Modification to the C.S.I.R.O. ark I Computer—B. E. Swire. (*Aust. J. ys.*, vol. 8, pp. 184–186; March, 1955.) he suggestion is put forward that a facility built into the machine for distinguishing tween machine commands and interpre-e or "hyper" commands so that the mer are performed directly while on re-ipt of one of the latter control is directed the head of the interpretation routine th simultaneous storage of the link datum enable return of control to the next pro-am command after performance of the perfunction. This would result in a con-lerable gain in speed. See also the articles Pearcey and Hill (Abstracts 640 and 641, oc. IRE, April, 1954.)

Courtesy of PROC. IRE and *Wireless Engineer*

56-40

Automatic Answering of Inquiries—L. E. iffith. (*Computers and Automation*, vol. 4, . 6–8; November, 1955.) Many organiza-ns which must provide answers to many utine questions a large number of times a y would be considerably aided by an tomatic question answering system. Such system could be extended to provide in-uctions for filling out forms and other ecialized applications. A machine in-nded for use in the Blue Cross home office described in this article. This particular achine involves the mechanical selection a particular record or tape which contains e answer to the desired question. This is an teresting application of known techniques; t it does not present any really new tech-ques.

G. Morrison

UTILIZATION OF DIGITAL EQUIPMENT

56-41

Stability of a Method of Smoothing in a gital Control Computer—William Karush. RANS. IRE, vol. EC-4, pp. 26–31; March, 55.) Real-time determination of position sed on sampled and noisy measurements is important task in navigation and guid-ce systems. It has long been recognized at the high-frequency noise of observa-ns can be smoothed by making use of ne well-established physical limitations of e moving objects. Since aerial vehicles ve reasonably predictable behaviors in locity, acceleration, etc., with the use of derivatives of position one can pre-calculate the next position sample. This predicted value is weighted in with the observed value, with the relative values of the weighting coefficients employed, indicating our relative credence in the prediction and observation respectively. When dealing with sampled data as one does in a digital control system, the computation of velocity and acceleration itself can be done in so many different ways, that one can just as well start with a clean sheet of thinking. One might as well talk about fitting a curve through a fixed number of previous samples to predict the new sample. In this process the velocity, acceleration and other derivatives do not need to appear explicitly, but the n-th derivative is implicitly considered if the present and n previous samples are made use of. At least two methods of smoothing have been analyzed exhaustively in the literature: one by Levinson (referred to in the article under review), and the other by Karush in the present article.

Levinson combines linearly n observed samples to get a new smoothed sample, while Karush combines linearly $n-1$ previous smoothed samples and only the latest observed sample to get a new smoothed sample. Levinson's method is inherently stable, because the observed values are bounded and so is, therefore, a linear combination of n observed values. The method discussed by Karush, however, can be unstable, as the new smoothed value is computed on the basis of old smoothed values which in turn were based on older smoothed values, and so on. The effect is cumulative and careless choice of parameters can lead to instability. (The reviewer notes without proof that this article's method can be far more effective for the same computational effort than Levinson's.) The first question Karush handles is stability. He uses classical prediction, wherein a polynomial is fitted through q previous smoothed samples. This prediction is weighted by $\alpha<1$, while the actual observation is weighted by $1-\alpha$. The limit on α as a function of q has been obtained by some neat and impressive mathematical juggling. The formula for α critical is one of the contributions of the article.

Karush has also obtained an expression, in effect, for the rms error (in the steady state) by getting the ratio of the variance of the smoothed data to that of the observed data. It is clear that this ratio should be less than one or else the noise has not been reduced by smoothing. Furthermore, the ratio should be minimized.

Karush has not considered these very important and practical questions. He could have probably shown—and if he had, his valuable article would have been even more valuable—that this ratio is always (with all α's giving stability) less than 1 for $q=1$ (linear prediction), may be $(0<\alpha<0.2)$ less than 1 for $q=2$ (parabolic prediction), and is *never* less than 1 for $q=3$. Thus the article fails to warn the reader *not* to use cubic prediction. The physical reason is that the prediction process itself introduces noise (being equivalent to taking derivatives), and that the noise so introduced is greater than the noise smoothed out. (The reviewer has not proved it, but suspects quite strongly that for $q>3$ the effect is even worse and the ratio does not get under 1 for any value of q. If so, only linear and parabolic predictions are of any practical use in this method of smoothing.)

Other methods not based on polynomial curve fitting, yet using previous smoothed samples, may offer greater promise for smoothing, but more difficulty in the analysis.

John M. Salzer

56-42

Automatic Coding for Digital Computers—G. M. Hopper. (*Computers and Automation*, vol. 4, pp. 21–24; September, 1955.) Most readers will recognize Dr. Hopper as one of the early pioneers in the field of automatic programming. In this particular article, she presents a thumbnail sketch of the history of this field from the first subroutines on the ENIAC to the A-series compilers now in operation.

G. Morrison

56-43

Automatic Programming: The A2 Compiler System, Part 1 and Part 2—Programming Research Section, Eckert Mauchly Division, Remington Rand. (*Computers and Automation*, vol. 4, pp. 25–29; September, 1955; pp. 15–27; October, 1955.) One of the compiling routines in widespread use today is the A2 compiler designed for the UNIVAC. The instruction manual for this compiler is reproduced in these two parts.

G. Morrison

56-44

A Big Inventory Problem and the IBM 702—Neil MacDonald. (*Computers and Automation*, vol. 4, pp. 6–12, 38; September, 1955.) The IBM 702 is an electronic computer intended for application to business problems. One category of business problem that requires mechanization is inventory control. In this article, the general characteristics of this machine are presented in condensed form. An example of the use of a machine with these characteristics on an inventory control problem is given in very general form.

G. Morrison

56-45

Automatic Digital Computers in Industrial Research. VI—R. F. Clippinger, B. Dimsdale, J. H. Levin. (*Jour. Soc. Industrial and Applied Math.*, vol. 3, pp. 80–89; June, 1955.) This article is the last in a set of six on the same subject (cf. Review 55-73, June, 1955.) In this article, the authors summarize the present situation with respect to: 1) applications of digital equipment to scientific and engineering problems; 2) data processing, conversion, manipulation and storage; 3) reliability of computers, their cost and size; 4) business applications in general. In addition, they make some predictions concerning these items during the next decade or so.

Thomas H. Southard

56-46

The Role of General Purpose Digital Computers in Automatic Control and Information Systems—Arnold Cohen. (*1954 IRE CONVENTION RECORD, Nat. Conv.*, Part 4, pp. 82–86.) The author sets down two criteria which he feels a general purpose

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ital computer must meet in order for it to able to fit properly into automatic con- l and other real time systems. These are: ether or not it can communicate effec- ely with other parts of the system; and ether or not it can process data fast ough for the application.

Mr. Cohen chooses the ERA 1103 com- ter as an example of a machine which believes will fill the above conditions for ny real-time control systems. In backing his contention, he describes the general ical arrangement of the machine and ex- ins that it has been designed so as to ve flexibility in external communication rough three powerful instructions, cal- lation proceeding during the functioning the terminal equipment.

He then goes on to show how the com- tational speed of the machine is much en- nced by the use of a so-called "repeat" in- ruction, which causes the next-following struction to be acted on a number of times ven in the repeat instruction. By example demonstrates the inherent simplicity, ing the repeat instruction, of the instruc- on chain required for such often needed erations as scalar product, block transfer, ctor product, linear smoothing, and radix nversion. Finally, he touches on the index mp instruction, which embodies in one mmand the tally modification, test, and nditional jump normally used to close a peated program loop.

The conclusion, which the author draws, that there do exist general purpose com- ters capable of reasonably satisfactory rformance in real-time systems. He feels at because they are available their use in eference to specially constructed machines ll be more economical.

Oliver Whitby

56-47

Use of a Computing Machine as a echanical Dictionary—Andrew D. Booth. *Nature*, vol. 176, p. 565; September 17, 55.) This "letter to the editor" briefly dis- sses the use of a digital computer to store dictionary for mechanical language trans- ion. In particular, the methods of search- g such a table are described. It is shown at it is time consuming to start simply at e end of the table and test each successive rd until the correct one is found. An in- val halving technique is more economical. a table of 10,000 words, any given word n be located in less than fourteen compari- ns.

D. E. Hart

2.6:671.142 56-48

Language Translation by Electronics: vel Application of Digital Computing achines—J. P. Cleave and B. Zacharov. *Wireless World*, vol. 61, pp. 433–435; Sep- nber, 1955.) The problem is discussed th particular reference to technical trans- ions into English.

Courtesy PROC. IRE and *Wireless Engineer*

56-49

Found—A "Lost" Moon—Paul Herget. *omputers and Automation*, vol. 4, pp. 10– ; November, 1955.) The University of ncinnati Observatory has been using NIVAC to compute celestial positions—an activity which could provide some interest- ing articles concerning computer applica- tion; however, this article, which is a reprint from an advertising publication, provides no information other than that the problem is very complex and that the computer is very much faster than the desk calculator.

G. Morrison

56-50

Linear Programming and Computers, Part I and Part II—Chandler Davis. (*Com- puters and Automation*, vol. 4, pp. 10–17; July, 1955: pp. 10–15; August, 1955.) Linear programming is a method of solution of problems in which the objective is the minimization or maximization of a linear function, the variables of which are re- stricted by a system of linear equalities and linear inequalities. The solution can be con- sidered a point in hyper space which is one of the extreme points of a hyper solid which is defined by the system of linear equalities and inequalities. The author illustrates by simple examples one method of determining the solution to this problem. Known as the simplex method, it provides a repetitive procedure for advancing from a randomly chosen extreme point through other extreme points to the one which gives the best value of the linear function and is therefore the solution.

G. Morrison

BOOK REVIEWS

56-51

Approximations for Digital Computers—Cecil Hastings, Jr. with Jeanne T. Wayward and James P. Wong, Jr. (Princeton Univer- sity Press, Princeton, N. J., vii×201 pp.; 1955.) This book contains two sections. The first section includes a discussion of such topics as best fit, linear weights, solution of equations, Tchebycheff polynomials, notes of convergence, choice of form, etc. Each topic is well illustrated by examples with brief and sometimes humorous personalized text. The second section consists of poly- nomial approximations of twenty-three often used functions. Approximations are given to various precision limits. Each approxima- tion is accompanied by a carefully drawn error curve and a comment as to the use of the approximation. The error curves are sometimes given in absolute value and at other times in relative value. The approxi- mations have been available in a very limited distribution for a few years, but have already been widely used in the computing field. All users of computing machines are anxious to reduce the size of a program, the number of instructions executed, and the corresponding computing time. The numeri- cal methods previously used were series ex- pansion or table look-up with various de- grees of interpolation. Mr. Hastings' ap- proximations require a minimum of comput- ing and storage space in a stored program machine, and are, therefore, very valuable. The book is not complete in that it does not describe other methods of approximation and curve fitting which are sometimes useful. The best fit as defined and used by Mr. Hastings produces the minimum of the absolute deviation. This book should be available to and read by all engineers who have the opportunity of working with digital computing machines.

G. T. Hunter
Courtesy of PROC. IRE

56-52

Automatic Feedback Control System Synthesis—John G. Truxal. (McGraw-Hill, New York, 675 pp., illus.; 1955.) This book is written as an advanced textbook on feed- back control systems. It presupposes con- siderable sophistication on the part of the reader, not only in the area of feedback control theory, but also in the use of Laplace transform techniques in transient analysis.

The major portion of the book is devoted to the first section, which is an outline of a straightforward method of designing linear feedback control systems to satisfy require- ments in terms of specified steady-state and transient response criteria. This method basically consists of the following proce- dures: relation of the system steady-state and transient response to the system closed loop transfer function and the resultant pole- zero location in the s domain; finding the corresponding open-loop transfer function and open loop pole-zero locations; and de- signing the series network which will force the system open loop transfer to take the required form by the process of adding to and cancelling poles and zeros of the func- tion resulting from the unalterable system elements.

The author assumes that the reader is familiar with frequency response techniques. However, since his primary purpose is to expound his approach to synthesis in terms of transient response, he devotes a minimum of space to frequency response methods. He discusses in some detail signal flow diagram methods of describing a system, RC net- work synthesis, root locus method, and de- sign by pole-zero configuration in the s plane. Two following chapters of the book discuss the application of statistical methods to the design of feedback systems. The pro- cedure preferred by the author is not so clearly indicated here as it was in the first section. However, this section does give the reader some insight into several somewhat different statistical approaches to the prob- lem of a feedback control system con- taminated by noise, and gives some idea of the nature of the mathematical methods frequently used in the statistical approach.

The next section is devoted to the dis- cussion of sampled-data systems and the Z-transform extension of the Laplace trans- form methods. This material serves as an introduction to the field of sampled-data systems. (However, much has been done in this area since this book went to the pub- lisher. The reader who wishes to become well informed on sampled-data systems is advised to seek out the current literature, particularly the articles by E. A. Jury pub- lished in the *AIEE Transactions* in the last year or so.)

The last portion of the book is a brief treatment of nonlinear systems. The more commonly used methods of attack—the describing function method of Kochen- burger, and the phase-plane method—are discussed. The concept of using phase-space methods for analysis of higher order systems is not brought out. It is of course possible to

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—*The Editor*

icize some details of this book. The hor sometimes assumes that the reader l quickly discern significant aspects of cepts scantily described in the text, and devotes space to resultant details when it ght have better been used in further de- opment of the basic concepts. An example ound in the development of the concept error constants at the end of the first pter. Two definitions are given: one for assical" error constants which are directly ted to the system steady-state error for ious forms of input, and the other for neralized" error constants which are cribed in terms of a McLauren's series ansion of the error ratio $E/R(s)$. It is ted that under certain given conditions "generalized" and "classical" forms of or constant are identical, but otherwise y are not. No other proof or demonstra- n of the relationship between the two ms is given. There is no discussion of the ge of values of s for which the McLauren's expansion of $E/R(s)$ is convergent. The author then devotes five pages to a detailed discussion of properties of the "generalized" error constants which are valid only if the McLauren's expansion is convergent over a wide range of values of s. It seems to the reviewer that much more could have been done to aid the reader if some of that space had been devoted to a more detailed discussion of the McLauren's expansion, its convergence, and the specific relation of its coefficients to the "classical" error coefficients. This is felt all the more strongly since the discussion of the synthesis method of Chapter Five starts with the use of the "generalized" error coefficients.

Chapter Three on the synthesis of RC networks is hard for the uninitiated to follow, and the reader will probably find himself hunting up the given references in order to master the topic. Perhaps the author's style here is a deliberate attempt to force the reader to the references cited, in recognition of the difficulty of including a volume on modern network theory in a volume on feedback control systems. The text is well larded with references which appear at the bottom of the page concerned. This location is convenient for immediate use but makes it harder to look up references later.

Overall, the book certainly represents a contribution to the literature on feedback control systems. The author must be congratulated for his coherent exposition of a method of linear design based on the required system response in the time domain. The sections on statistical methods, sampled-data systems, and nonlinear systems are brief when compared to the transient-response design section, but they serve to round out the book. The section on statistical methods should be of particular interest to those with no great previous knowledge in this area.

A. M. Hopkin

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IRE Transactions on Electronic Computers

Index to Volume EC-4—1955

Contents

Index to Authors

Numbers refer to index numbers in contents listing

Index to Technical Subjects